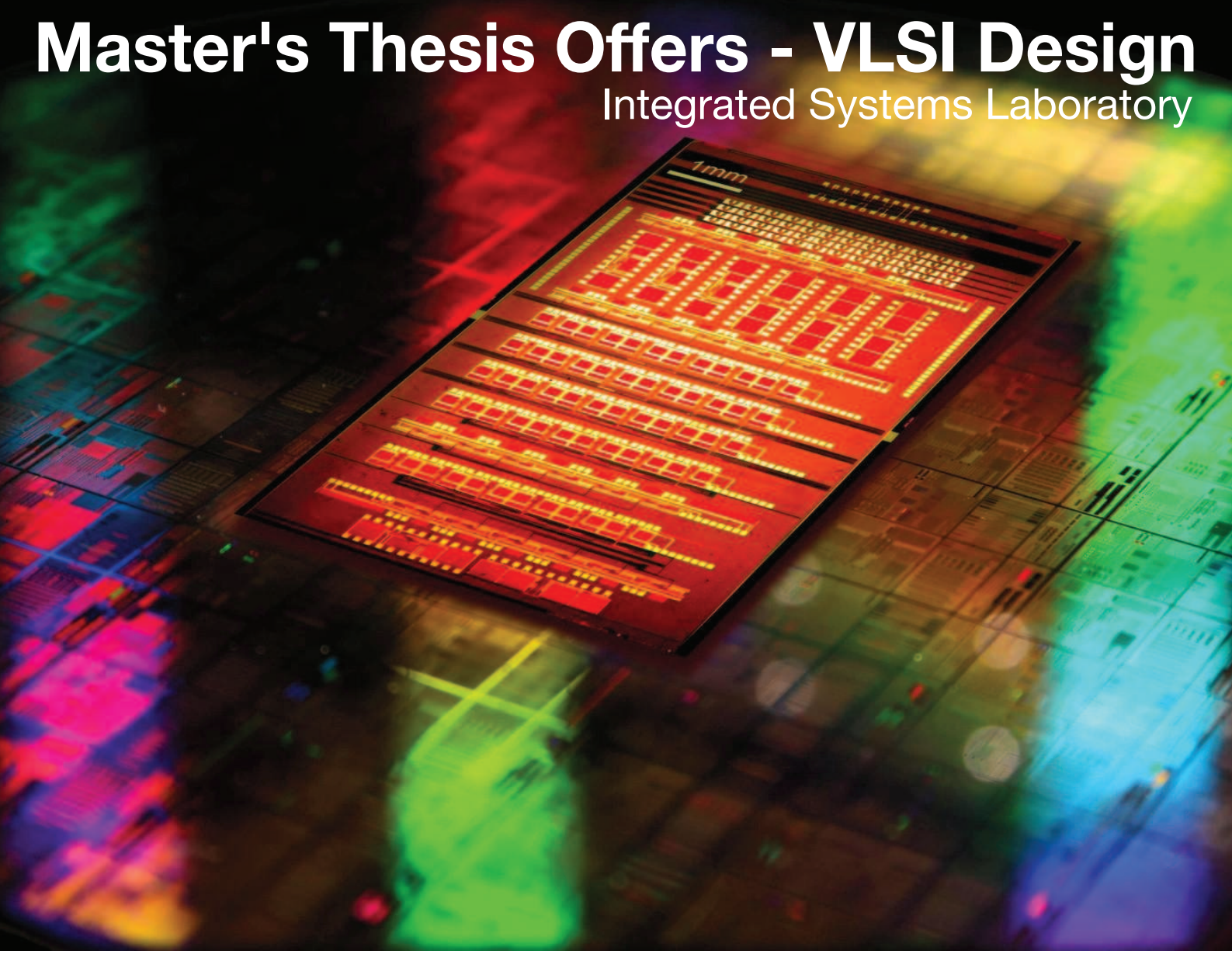
Master's Thesis Offers - VLSI Design

Integrated Systems Laboratory



CMOS integrated circuits manufactured with nanometer technologies are subject to numerous uncertainties due to second order effects that previously could be neglected but now actually limit the ultimate performance of the circuit and manufacturing yield. Such is the case of process variations, aging, and fluctuations in operating conditions (voltage drops, hot spots, radiation failures). For this reason we are working on design techniques that harden the circuit against these effects and incorporate multiple sensors that provide information about key parameters that can impact the final performance of the circuit.

This call gives you the opportunity to develop your master's thesis in this field.

Topics:

- Full-custom design of sensors in nanoscale technologies.
- Strategies for aging hardening in nanoscale technologies.
- Strategies for radiation hardening in integrated circuits.
- Design of sense amplifiers in nanoscale technologies.
- Verification in nanometric technologies with SystemVerilog and UVM.

What we offer:

Joining an active and internationally recognized research group.

Introduction to scientific and technological research methodology.

Access to advanced technologies and professional software

Possibility of sending the results of the thesis to an international scientific conference.

Possibility of manufacturating your designs.

What we look for:

Motivated, independent and creative students.

Training in full-custom design and / or VHDL.

Contact: pituero@die.upm.es

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