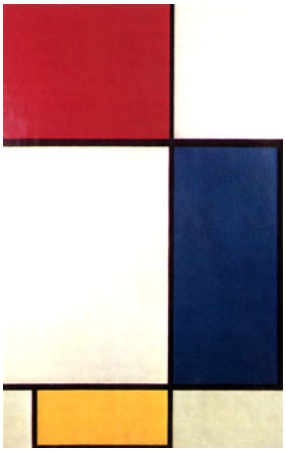
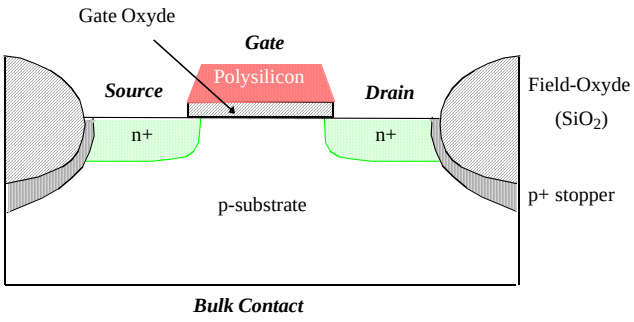
The Devices

Jan M. Rabaey

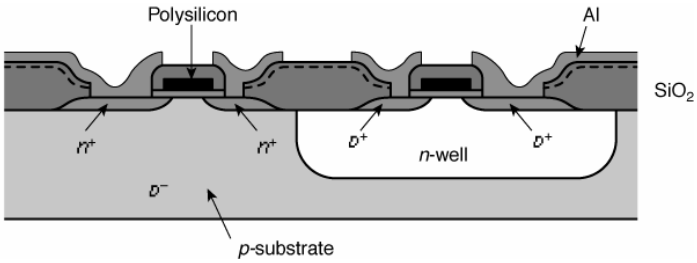


The MOS Transistor

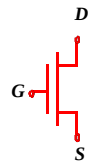


CROSS-SECTION of NMOS Transistor

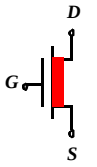
Cross-Section of CMOS Technology



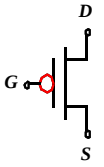
MOS transistors Types and Symbols



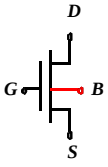
NMOS Enhancement



NMOS Depletion

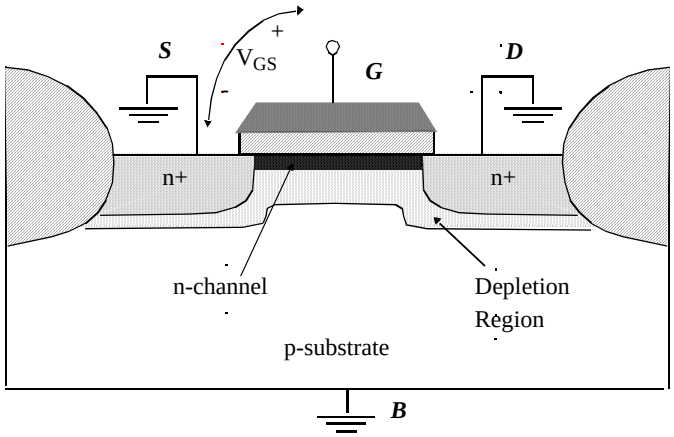


PMOS Enhancement

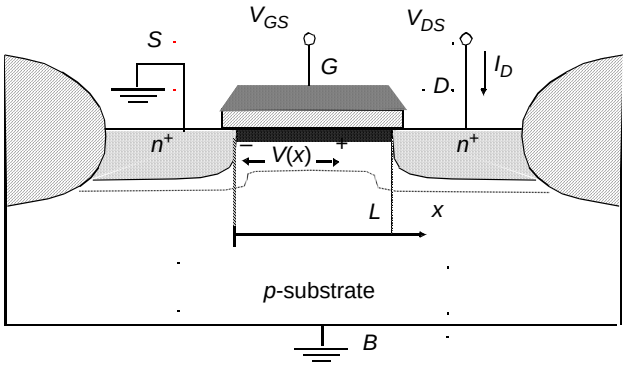


NMOS with Bulk Contact

Threshold Voltage: Concept



Current-Voltage Relations



MOS transistor and its bias conditions

Current-Voltage Relations

Linear Region: $V_{DS} \le V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

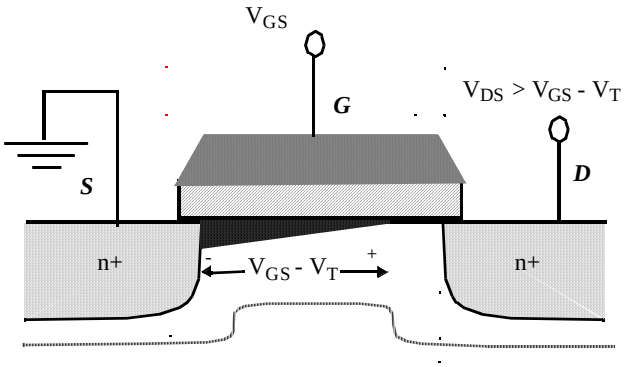
Process Transconductance Parameter

Saturation Mode: $V_{DS} \ge V_{GS} - V_T$

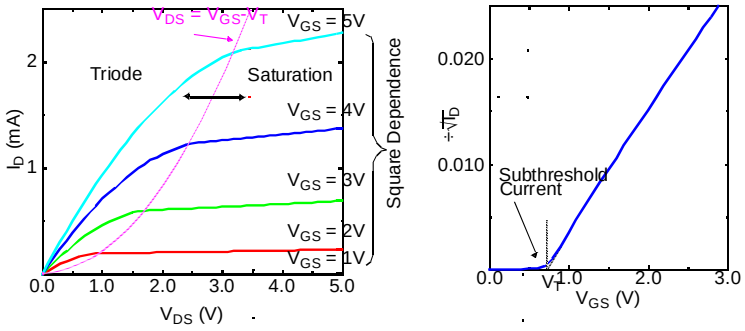
Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Transistor in Saturation



I-V Relation

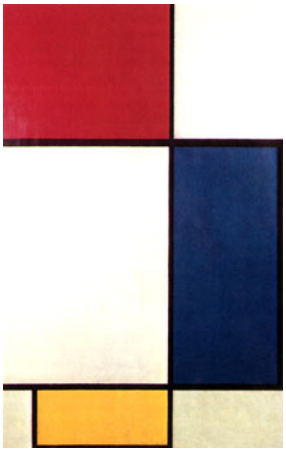


(a) I_D as a function of V_{DS}

(b) $\sqrt{I_D}$ as a function of V_{GS} (for V_{DS} = 5V)

NMOS Enhancement Transistor: W = 100 μm, L = 20 μm

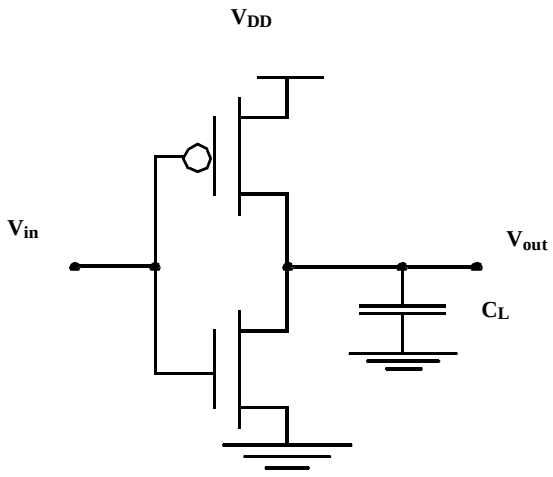
CMOS INVERTER



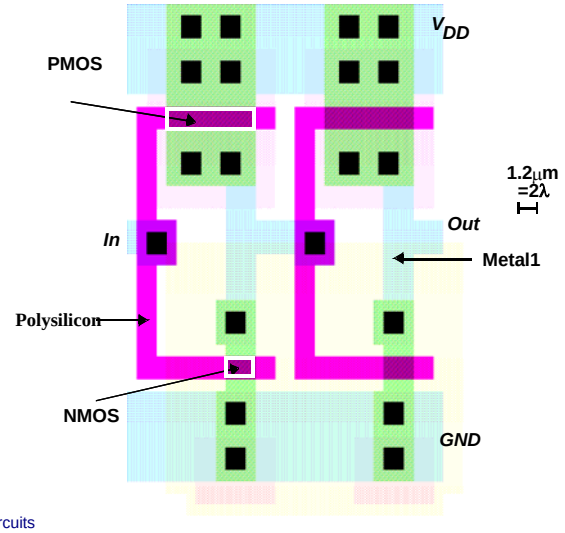
DIGITAL GATES
Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
  - » Speed (delay)
  - » Power Consumption
  - » Energy

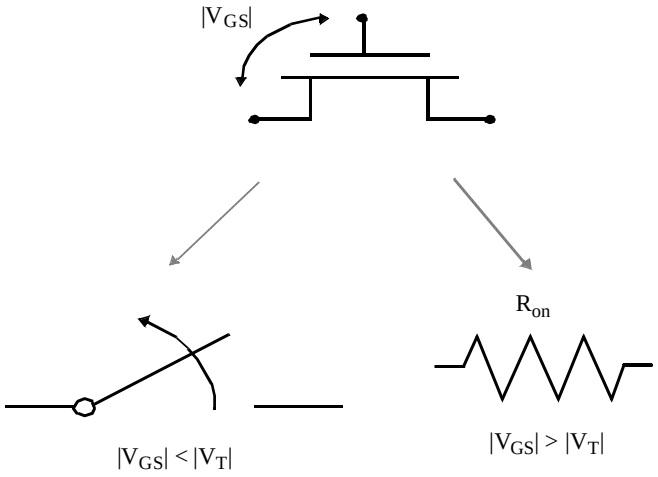
The CMOS Inverter:
A First Glance



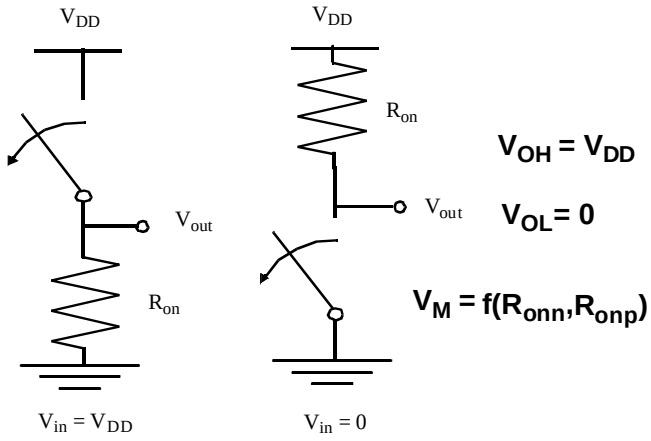
CMOS Inverters



Switch Model of CMOS Transistor



CMOS Inverter: Steady State Response

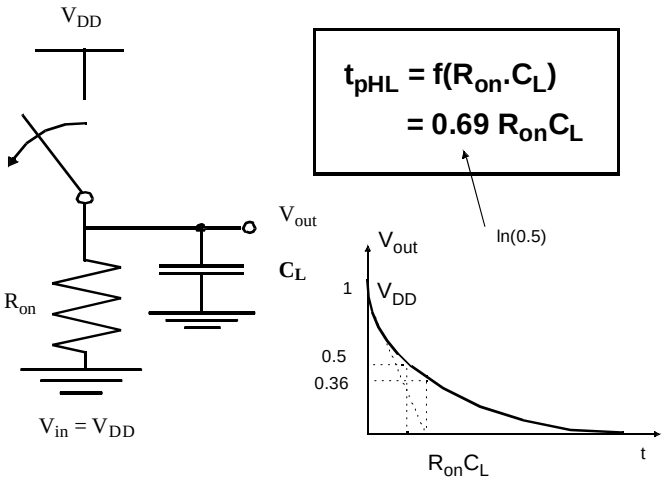


$V_{OH} = V_{DD}$

$V_{OL} = 0$

$V_M = f(R_{onn}, R_{onp})$

CMOS Inverter: Transient Response



$t_{pHL} = f(R_{on}.C_L)$

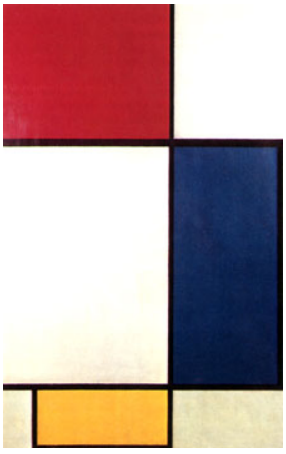
$= 0.69\ R_{on}C_L$

ln(0.5)

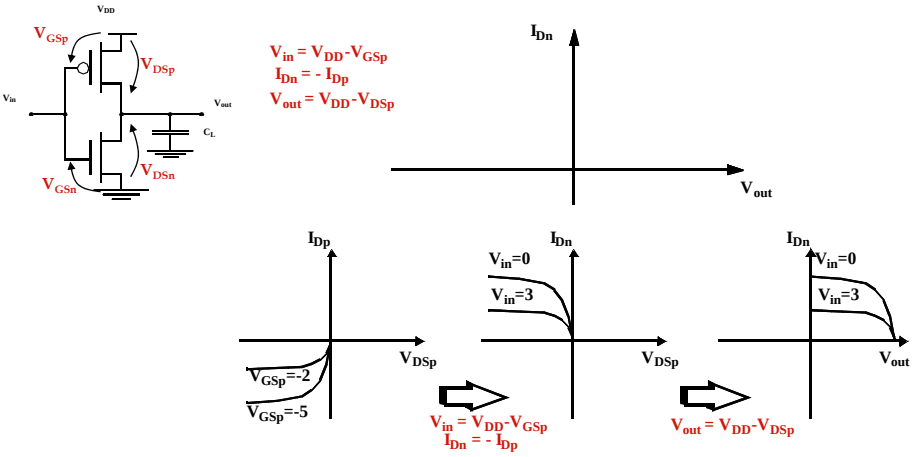
CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

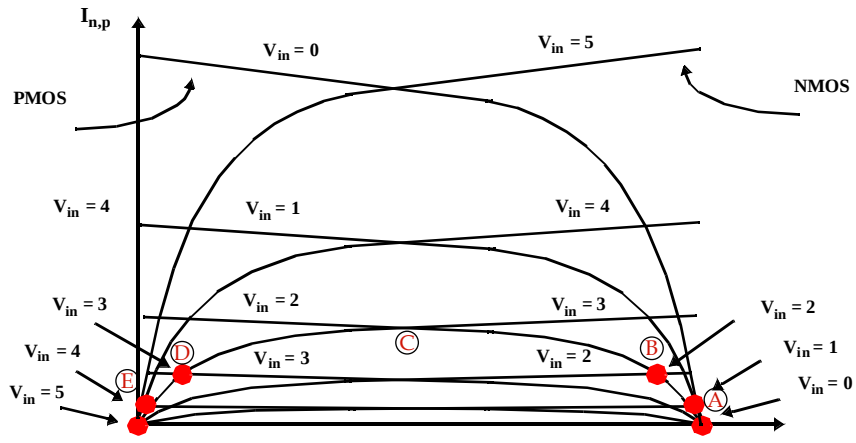
Voltage Transfer Characteristic



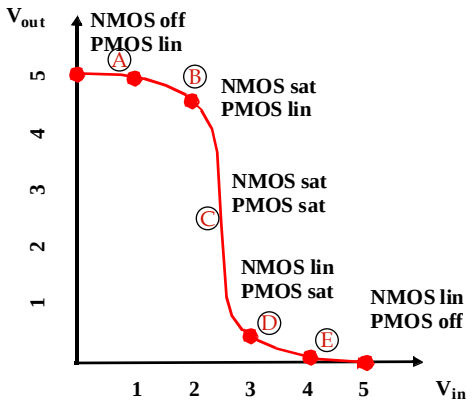
PMOS Load Lines



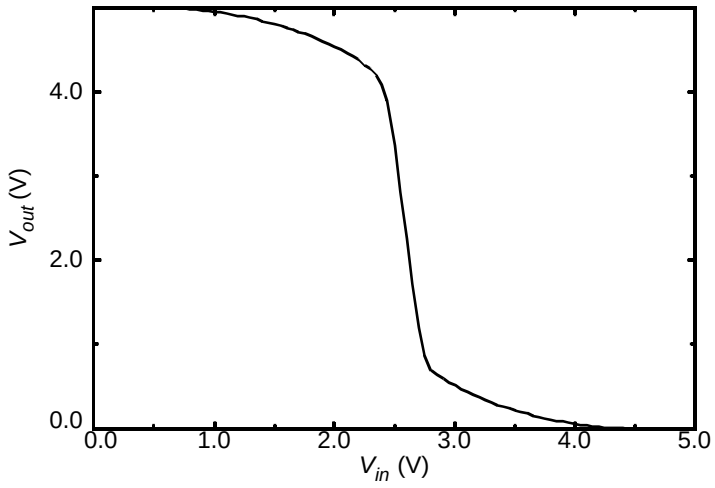
CMOS Inverter Load Characteristics



CMOS Inverter VTC



Simulated VTC



Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

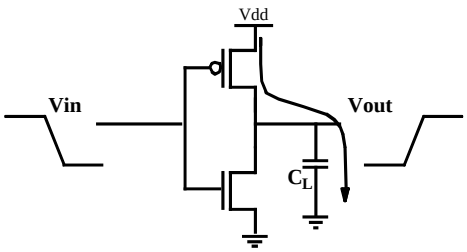
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Dissipation



Energy/transition = $C_L * V_{dd}^2$

Power = Energy/transition * f = $C_L * V_{dd}^2 * f$

- **Not a function of transistor sizes!**
- **Need to reduce C_L, V_{dd}, and f to reduce power.**