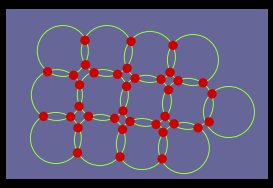
# EGE535 Low Power VLSI Design

## Lecture #2

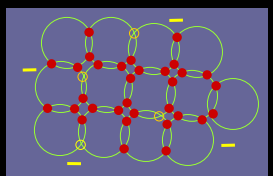
# MOSFET Basics



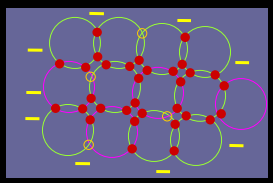
## Intrinsic and extrinsic Semiconductors



Intrinsic semiconductor
(no carriers at $0^0$ K)

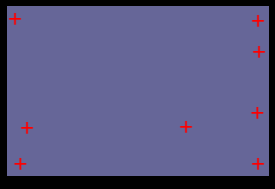


Intrinsic semiconductor
($n_i = p_i$ at room temp )



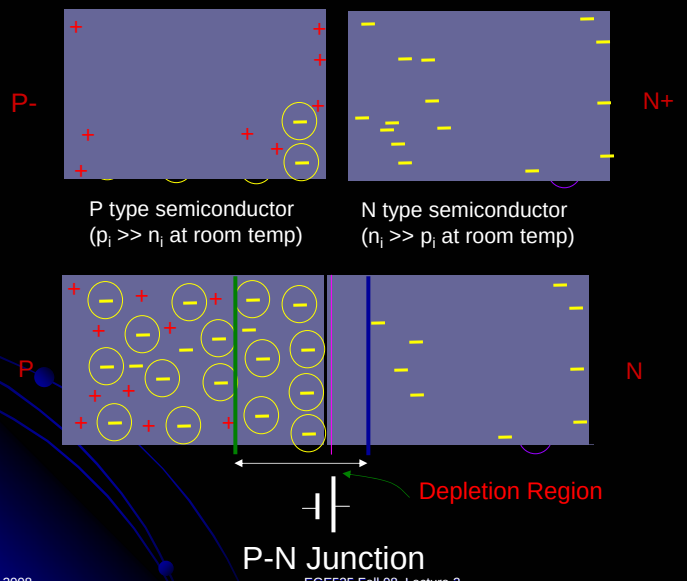
N type semiconductor
($n_i >> p_i$ at room temp)

N type semiconductor
($n_i >> p_i$ at room temp)



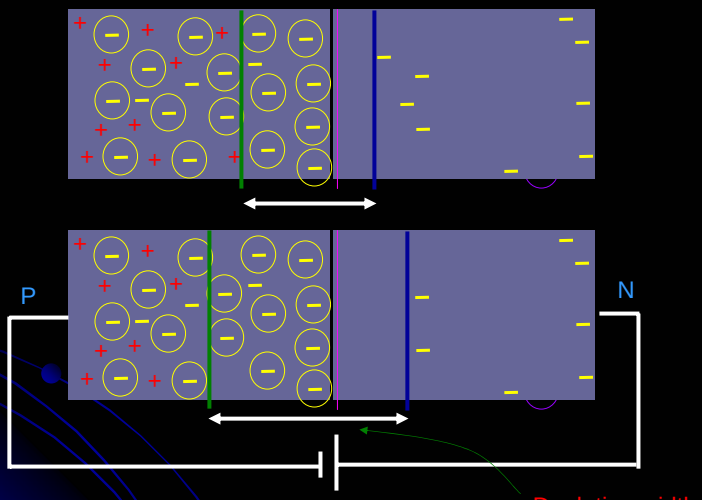
P type semiconductor
($p_i >> n_i$ at room temp)

# PN Junction

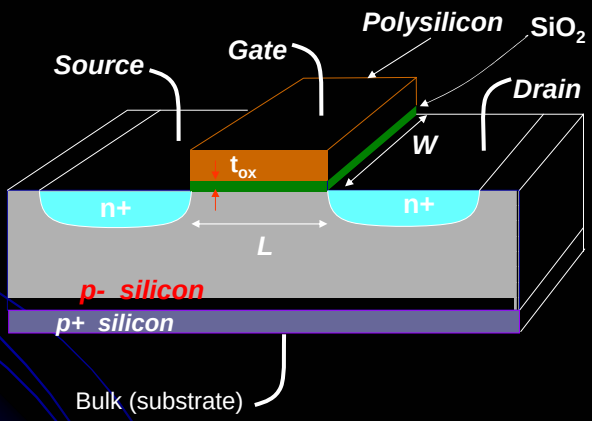





# PN Junction – Reverse Biasing

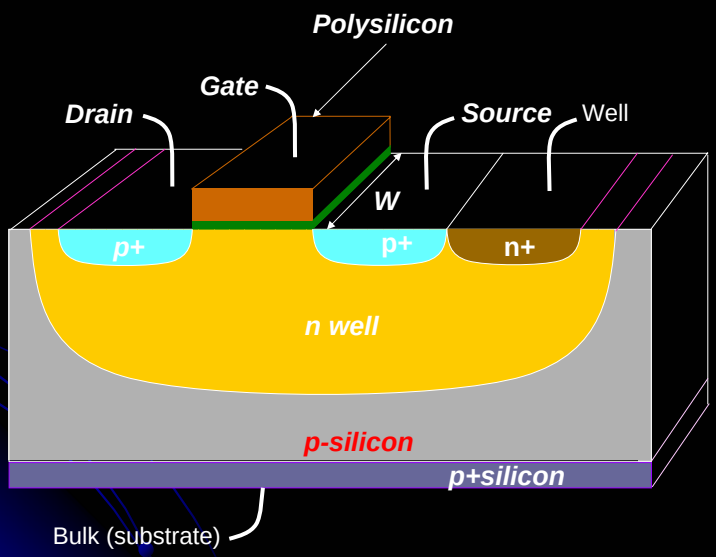


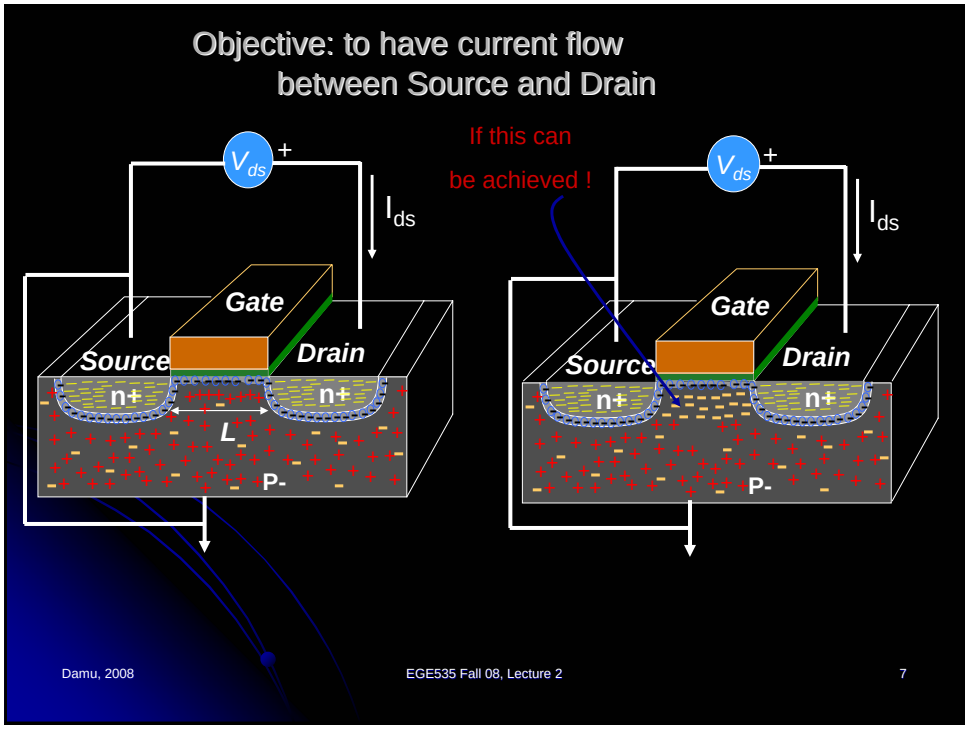
# nMOSFET






# pMOSFET




Objective: to have current flow
between Source and Drain
If this can
be achieved !
$V_{ds}$
+
$I_{ds}$
Gate
Source
Drain
n+
n+
L
P-
$V_{ds}$
+
$I_{ds}$
Gate
Source
Drain
n+
n+
P-
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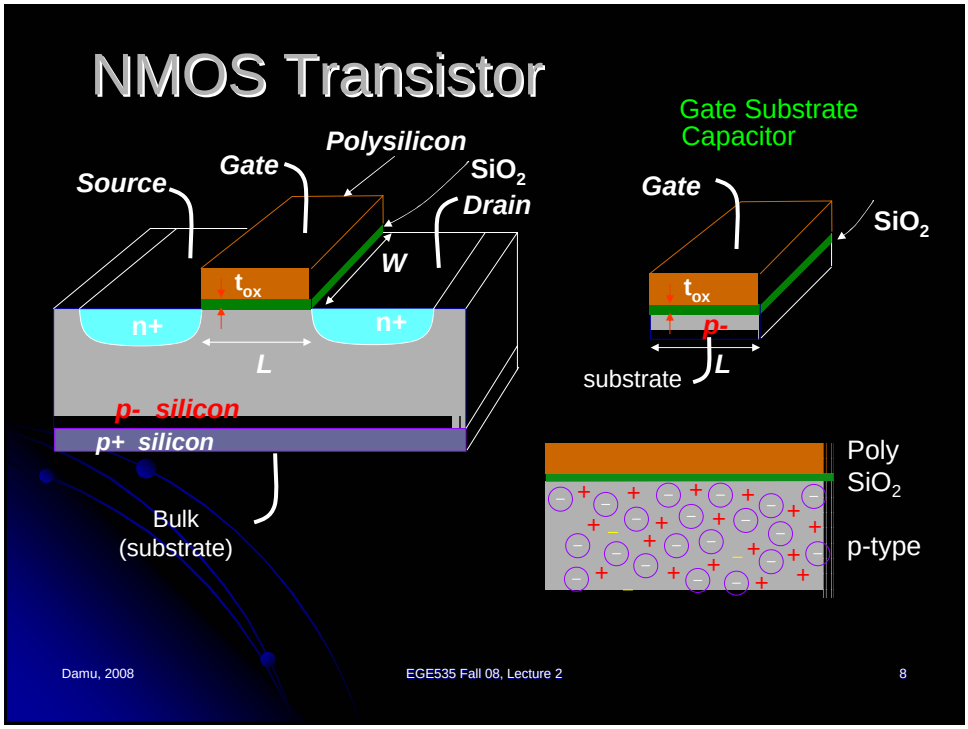
NMOS Transistor
Polysilicon
Gate
$SiO_2$
Source
Drain
W
$t_{ox}$
n+
n+
L
p- silicon
p+ silicon
Bulk
(substrate)
Gate Substrate
Capacitor
Gate
$SiO_2$
$t_{ox}$
p-
substrate
L
Poly
$SiO_2$
p-type
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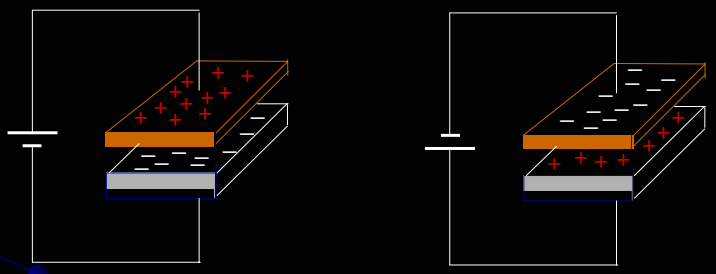
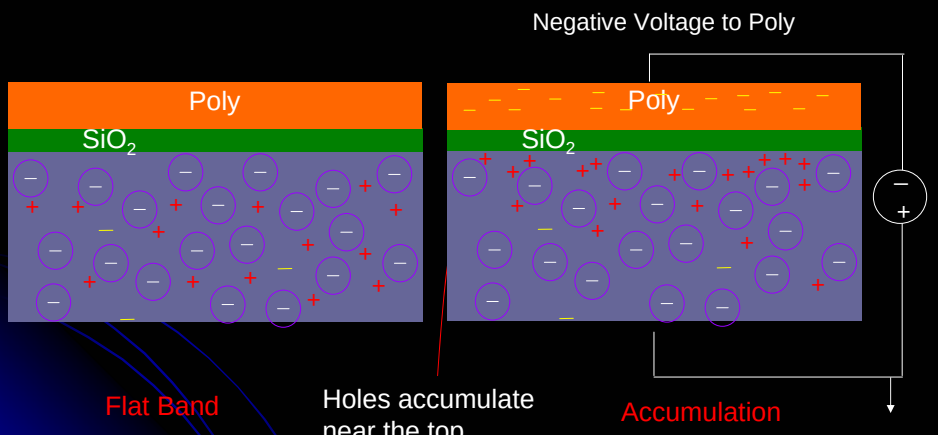
# Capacitor Charging



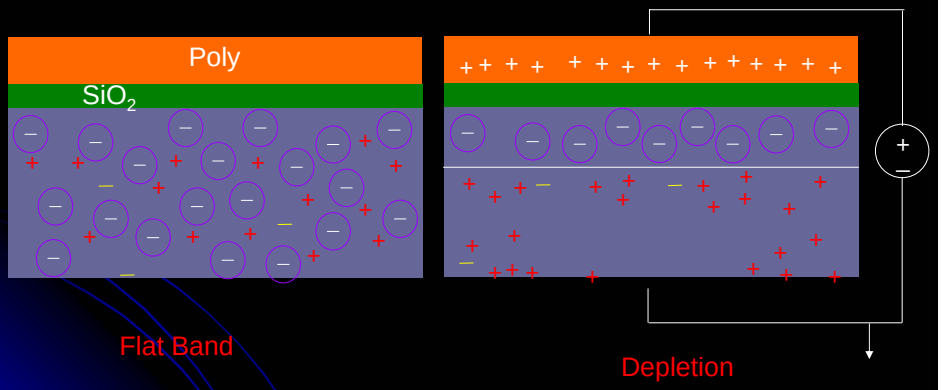


# The MOS Capacitor



# The MOS Capacitor

Very Small Positive Voltage to Poly




Flat Band

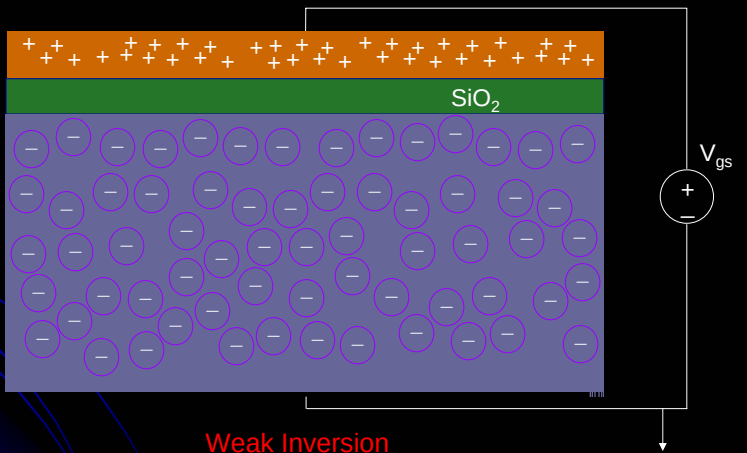
Depletion



# The MOS Capacitor

Small Positive Voltage to Poly

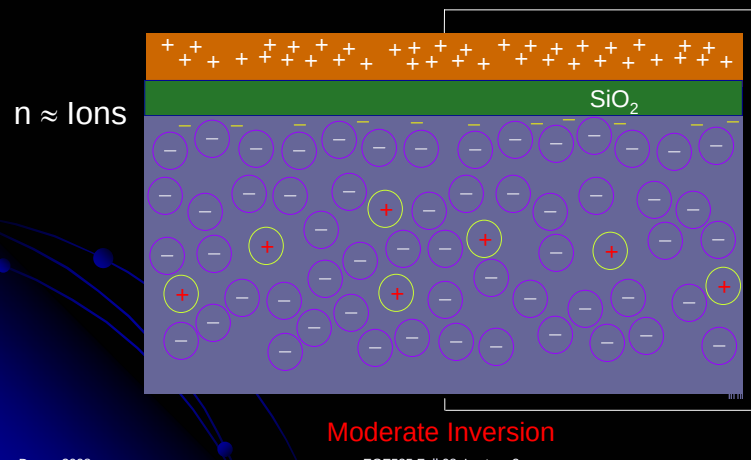
n << Ions




Weak Inversion

# Threshold Voltage $V_{th}$

**More Positive Voltage to Poly** $V_{gs} = V_{th}$

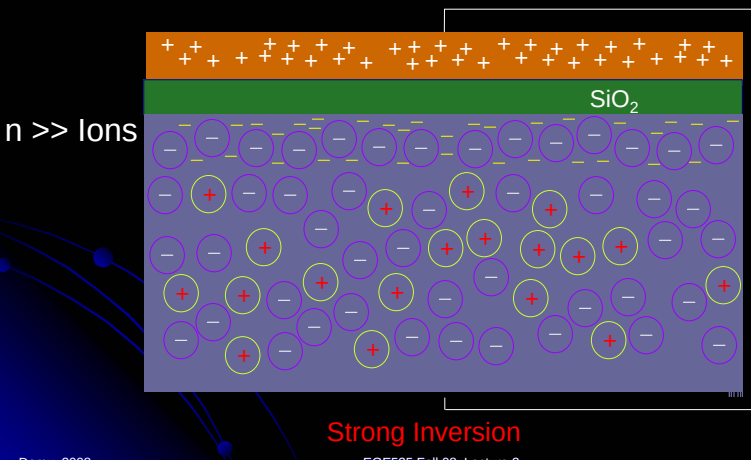



Moderate Inversion



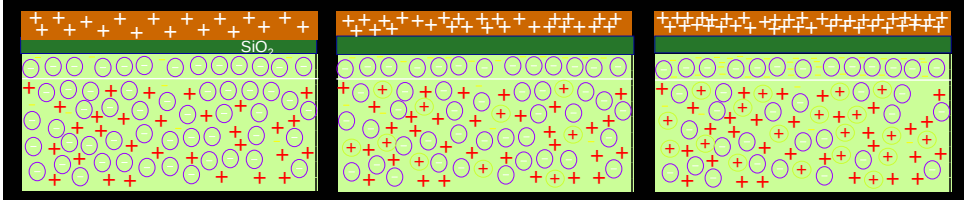
# Strong Inversion

**Much More Positive Voltage** $V_{gs} >> V_{th}$




Strong Inversion

# Threshold Voltage $V_{th}$




Weak Inversion
n<< Ions
$V < V_{th}$

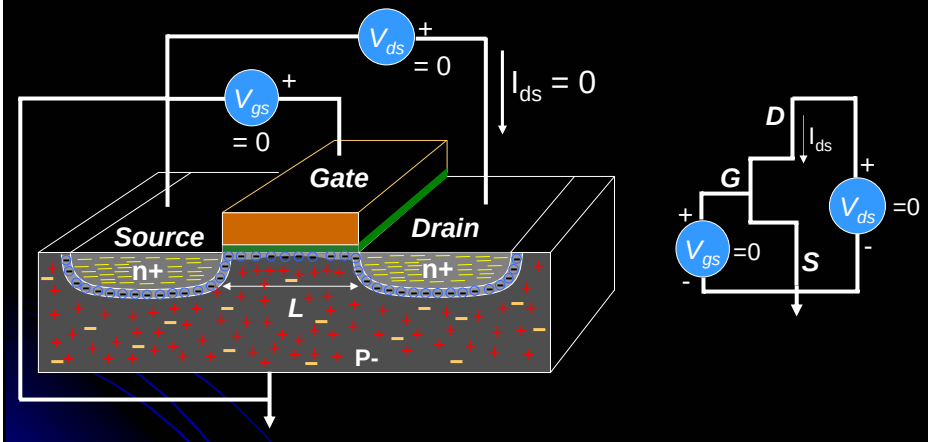
Moderate inversion
n ≈ Ions
$V = V_{th}$

Strong inversion
n >> Ions
$V >> V_{th}$

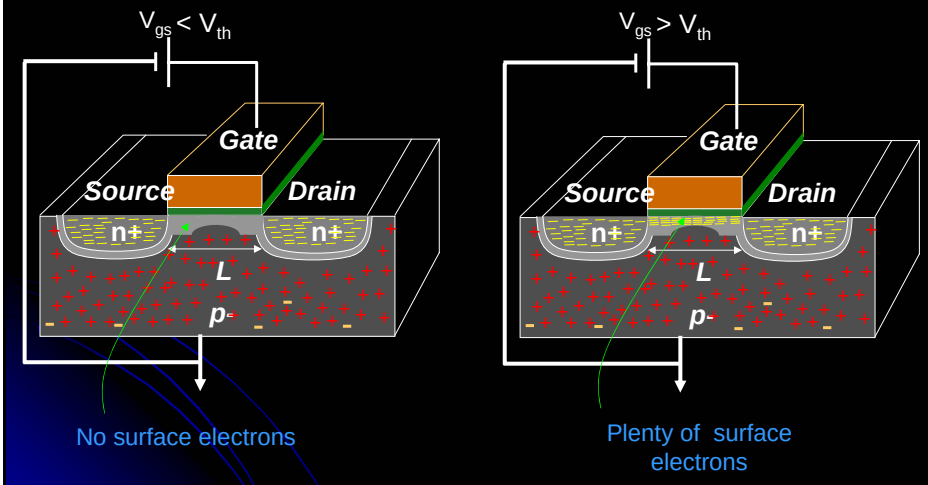
$V_{th}$ Minimum Voltage for Inversion



# Cutoff: $I_{ds} = 0$



# First Approximation: Threshold Voltage

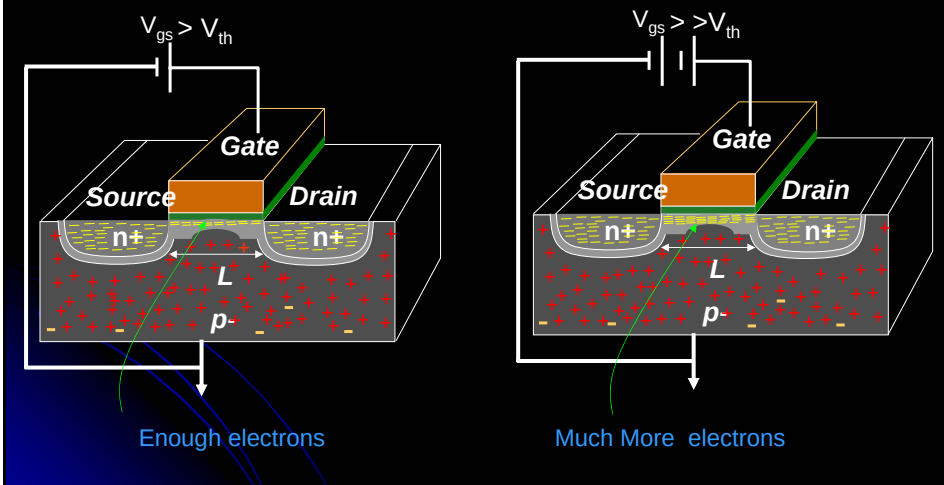



No surface electrons

Plenty of surface electrons



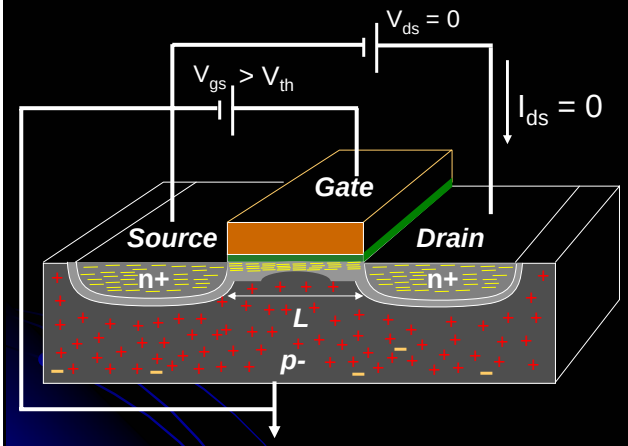
# Surface Charge with $V_{gs}$

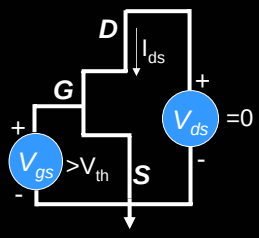



Enough electrons

Much More electrons

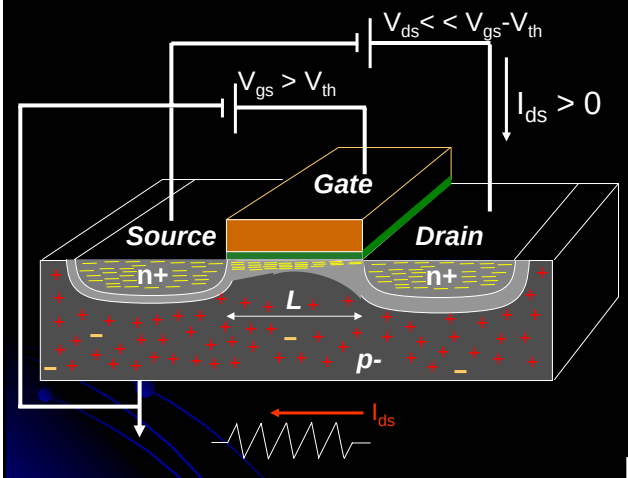
# Cutoff: $I_{ds} = 0$

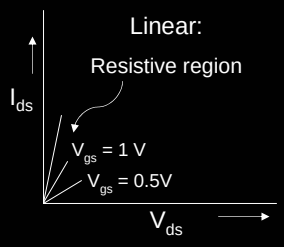





# Linear: $I_{ds}$ increases with $V_{ds}$



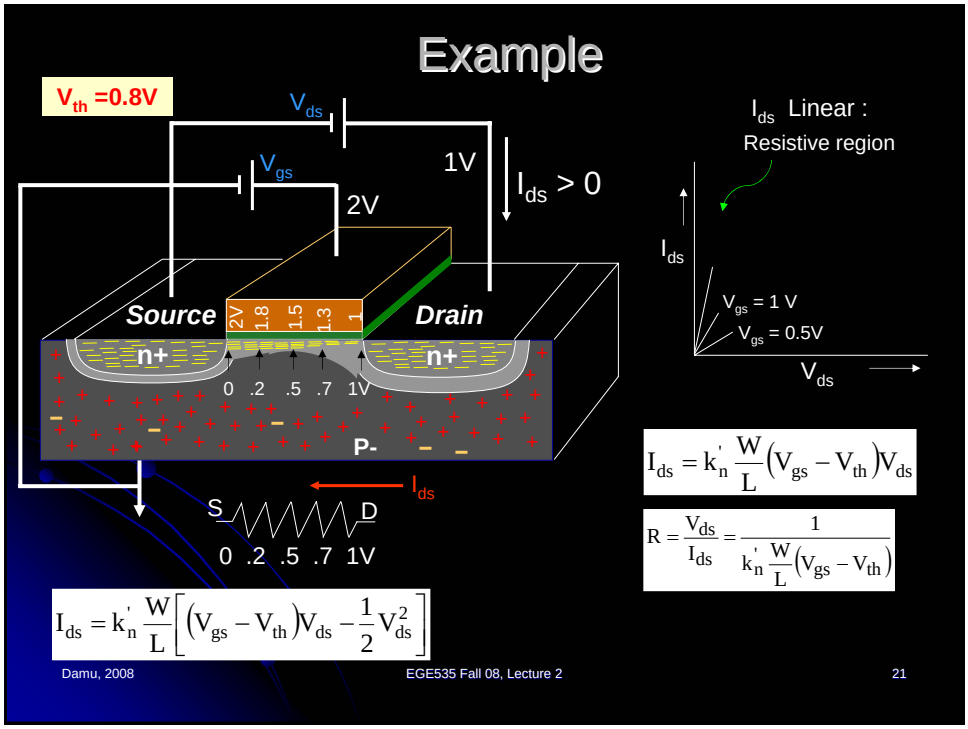




$V_{ds} << 2(V_{gs} - V_{th})$

⇨ Neglect $V_{ds}^2$

$$I_{ds} = k_n' \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

$$I_{ds} = k_n' \frac{W}{L}(V_{gs} - V_{th})V_{ds}$$


Example
$V_{th}$ =0.8V
$V_{ds}$
$V_{gs}$
1V
2V
$I_{ds}$ > 0
Source
Drain
n+
n+
P-
2V 1.8 1.5 1.3 1
0 .2 .5 .7 1V
$I_{ds}$
S
D
0 .2 .5 .7 1V
$I_{ds}$ Linear :
Resistive region
$I_{ds}$
$V_{gs}$ = 1 V
$V_{gs}$ = 0.5V
$V_{ds}$
$I_{ds} = k_n' \frac{W}{L}\left(V_{gs} - V_{th}\right)V_{ds}$
$R = \frac{V_{ds}}{I_{ds}} = \frac{1}{k_n' \frac{W}{L}\left(V_{gs} - V_{th}\right)}$
$I_{ds} = k_n' \frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]$
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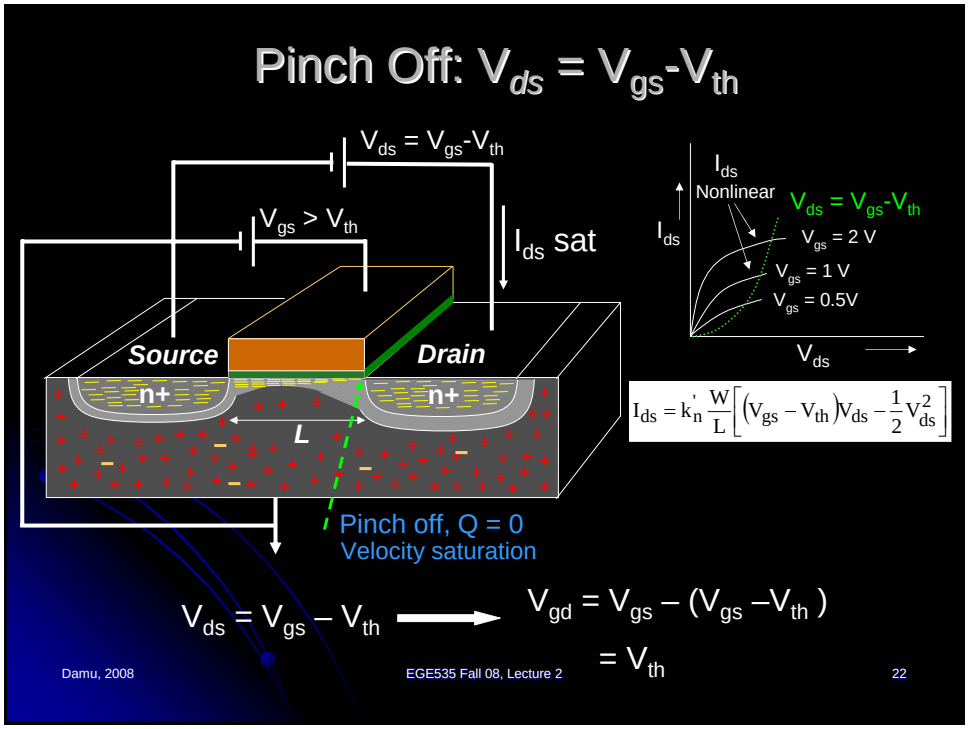
Pinch Off: $V_{ds} = V_{gs}$-$V_{th}$
$V_{ds} = V_{gs}$-$V_{th}$
$V_{gs} > V_{th}$
$I_{ds}$ sat
Source
Drain
n+
n+
L
Pinch off, Q = 0
Velocity saturation
$I_{ds}$
Nonlinear
$V_{ds} = V_{gs}$-$V_{th}$
$V_{gs}$ = 2 V
$V_{gs}$ = 1 V
$V_{gs}$ = 0.5V
$V_{ds}$
$I_{ds} = k_n' \frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]$
$V_{ds} = V_{gs} - V_{th}$
$V_{gd} = V_{gs} - (V_{gs} - V_{th})$
$= V_{th}$
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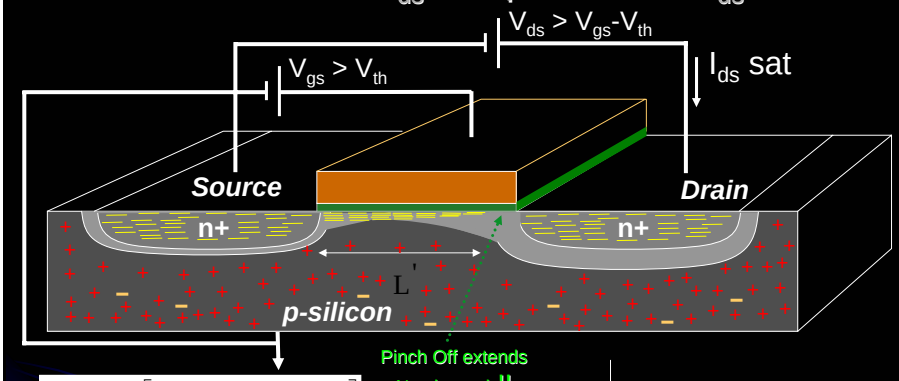
## Saturation: $I_{ds}$ independent of $V_{ds}$



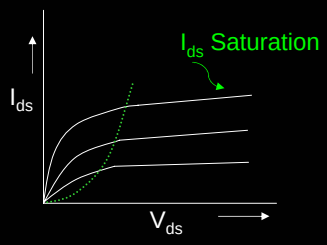

Pinch Off extends
No channel !!

$$I_{ds} = k_n' \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

For $V_{ds} > V_{gs}-V_{th}$ ⇒ Vds = Vgs-$V_{th}$

Velocity saturation: $I_{ds}$ constant

$$I_{ds} = \frac{1}{2}k_n' \frac{W}{L}(V_{gs} - V_{th})^2$$






## Regions of Transistor Operation

1. **Linear region :** $V_{GS} > V_{th}$ $V_{DS} < V_{GS} - V_{th}$

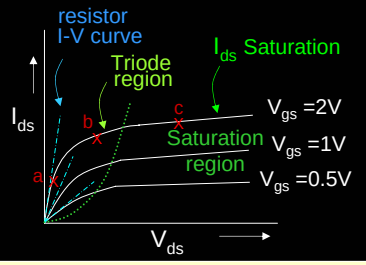
$V_{th}$ - threshold voltage

$$I_{ds} = k_n' \frac{W}{L}(V_{gs} - V_{th})V_{ds}$$

Deep Triode

$$R = \frac{V_{ds}}{I_{ds}} = \frac{1}{k_n' \frac{W}{L}(V_{gs} - V_{th})}$$

$$I_{ds} = k_n' \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$ Triode




2. **Saturation region:**

$V_{GS} > V_{th}$ $V_{DS} \geq V_{GS} - V_{th}$

$$I_{ds} = \frac{1}{2}k_n' \frac{W}{L}(V_{gs} - V_{th})^2$$

At "a" $$R = \frac{V_{ds}}{I_{ds}} = \frac{1}{k_n' \frac{W}{L}(V_{gs} - V_{th})}$$

At "b" $$R = \frac{V_{ds}}{I_{ds}} = \frac{1}{k_n' \frac{W}{L}\left[(V_{gs} - V_{th}) - \frac{1}{2}V_{ds}\right]}$$

At "c" $$R = \frac{V_{ds}}{I_{ds}} = \frac{2V_{ds}}{k_n' \frac{W}{L}\left[(V_{gs} - V_{th})^2\right]}$$

# Current Equation

$$I_{ds} = k_n' \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right] \qquad \frac{W}{L} - \text{Aspect ratio}$$

$k_n' = \mu_n C_{ox}$ – Process Transconductance

$\mu_n$ – Mobility of surface electrons

$C_{ox}$ – Gate Capacitance / Unit area

$C_{ox} = \frac{\varepsilon}{t_{ox}}, \quad \varepsilon = \varepsilon_0 \varepsilon_r$ Permitivity of $S_iO_2$

$\varepsilon_r$ Relative permitivity $= 3.9$

$\varepsilon_0$ Permitivity of freespace $= 8.854\times10^{-14}$ F/cm

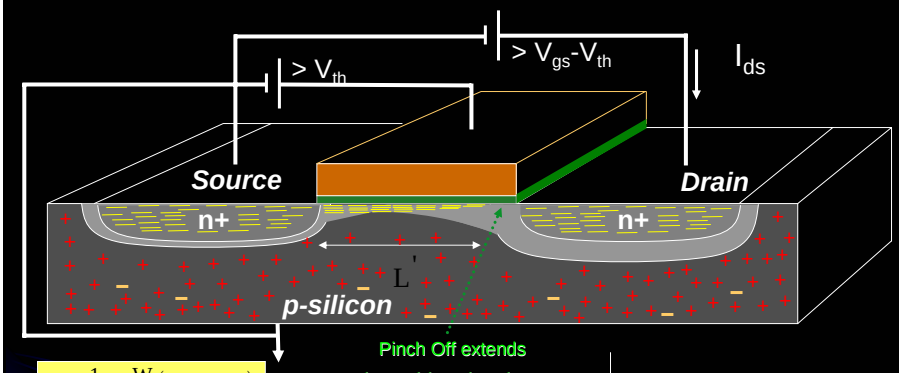
$t_{ox}$ Gate Oxide thickness $\approx 200^0 = 20$nm

$\beta_n = k_n' \frac{W}{L}$ – Device transconductance

$C_{ox} = 1.725 \text{fF}/\mu\text{m}^2$



# Channel Length Modulation



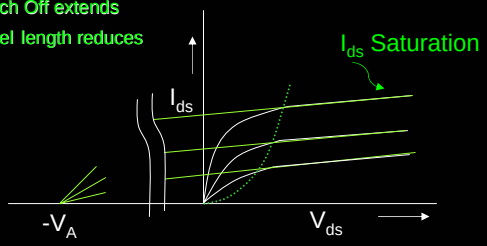

$$I_{ds} = \frac{1}{2}k_n' \frac{W}{L}(V_{gs} - V_{th})^2$$

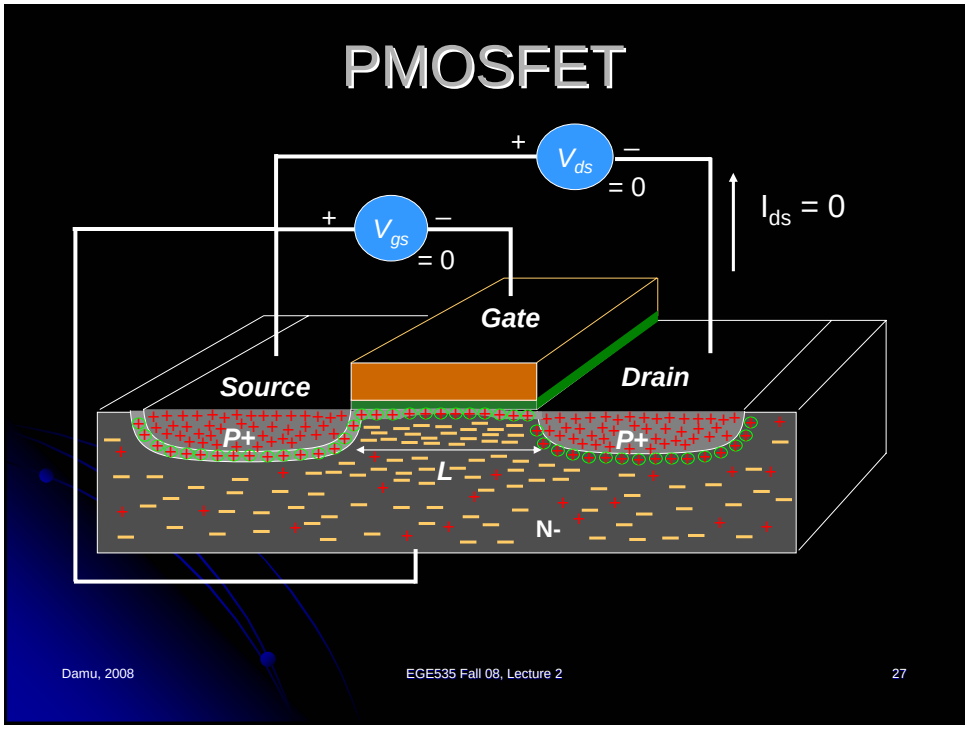
$$I_{ds} = \frac{1}{2}k_n' \frac{W}{L}(V_{gs} - V_{th})^2\left(1 + \frac{V_{ds}}{V_a}\right)$$

$$I_{ds} = \frac{1}{2}k_n' \frac{W}{L}(V_{gs} - V_{th})^2(1 + \lambda V_{ds})$$

$0.005 \le \lambda \le 0.02 V^{-1}$

Pinch Off extends channel length reduces




PMOSFET
+
$V_{ds}$
–
= 0
$I_{ds}$ = 0
+
$V_{gs}$
–
= 0
Gate
Source
Drain
P+
P+
L
N-
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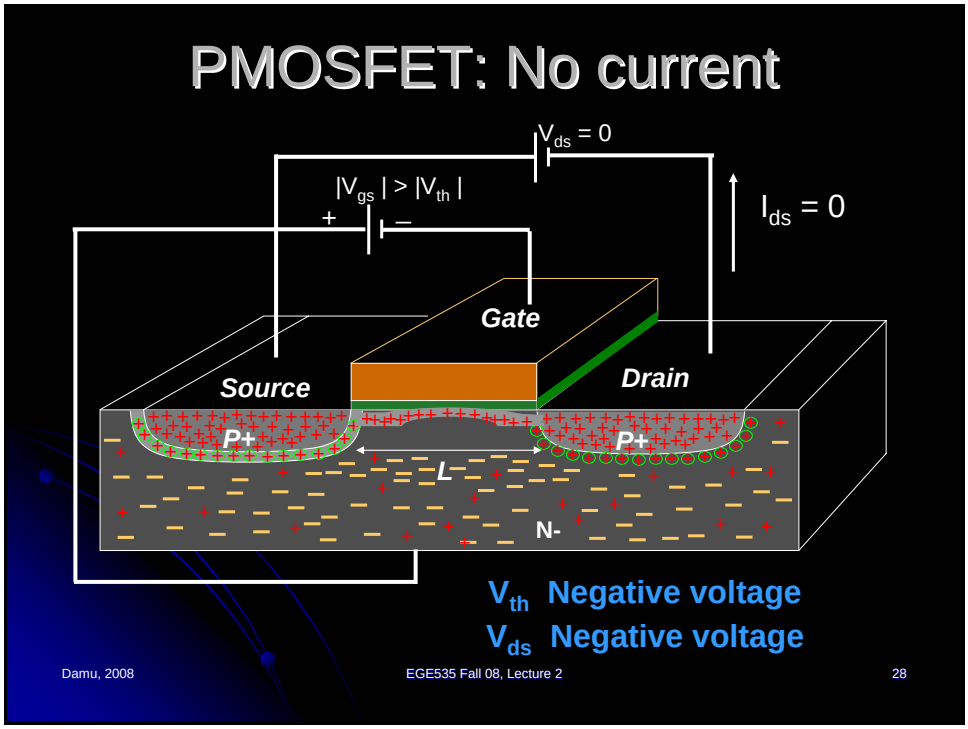
PMOSFET: No current
$V_{ds}$ = 0
$|V_{gs}| > |V_{th}|$
+
–
$I_{ds}$ = 0
Gate
Source
Drain
P+
P+
L
N-
$V_{th}$ Negative voltage
$V_{ds}$ Negative voltage
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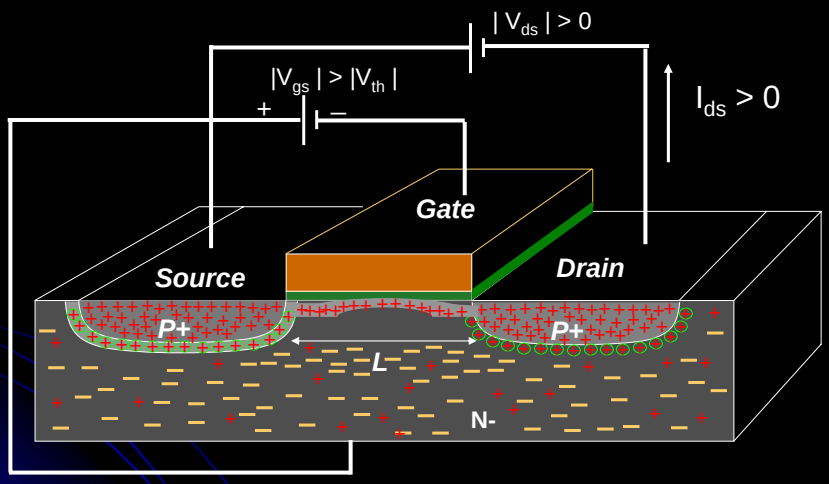
# PMOSFET: Current flow




$V_{gs}$ & $V_{ds}$ Negative voltages



# PMOS Transistor

1. Linear region : $|V_{GS}| > |V_{th}|$

$V_{th}$ - threshold voltage (Min for inversion layer)

$$I_{ds} = k_n' \frac{W}{L}(V_{gs} - V_{th})V_{ds}$$

$|V_{DS}| << |V_{GS} - V_{th}|$ Deep Triode

$$I_{ds} = k_n' \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

$|V_{DS}| < |V_{GS} - V_{th}|$ Triode

2. Saturation region: $|V_{GS}| > |V_{th}|$

$$I_{ds} = \frac{1}{2}k_n' \frac{W}{L}(V_{gs} - V_{th})^2$$

$|V_{DS}| \geq |V_{GS} - V_{th}|$

# MOSFET Symbols