POLITÉCNICA

"Ingeniamos el futuro"

Transistores CMOS

Pablo Ituero – MCRE – Octubre 2013

Departamento de Ingeniería Electrónica

Clase de hoy

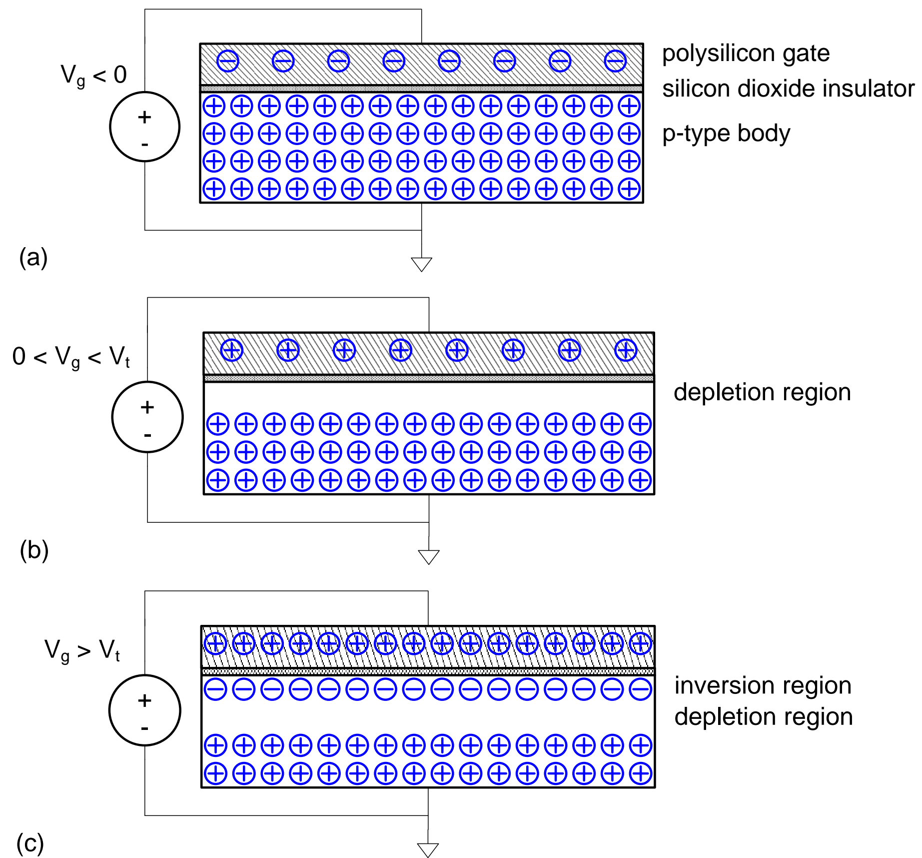
- Presentación intuitiva del funcionamiento
- Ecuaciones del modelo ideal
- Efectos de segundo orden
- Modelo unificado
- Procedimiento de análisis
- Ejercicios

Lecturas y fuentes de la presentación

- Lecturas:
  - Weste-Harris: CMOS VLSI Design
    - 2.1, 2. 2, 2.4.1-2.4.3
  - Rabaey: Digital Integrated Circuits
    - 3.3 hasta el modelo unificado
- Fuentes de transparencias
  - Weste-Harris: CMOS VLSI Design
  - Rabaey: Digital Integrated Circuits
  - Transparencias del curso EGE535 Low Power VLSI Design de la State University of New York
  - http://en.wikipedia.org/wiki/MOSFET

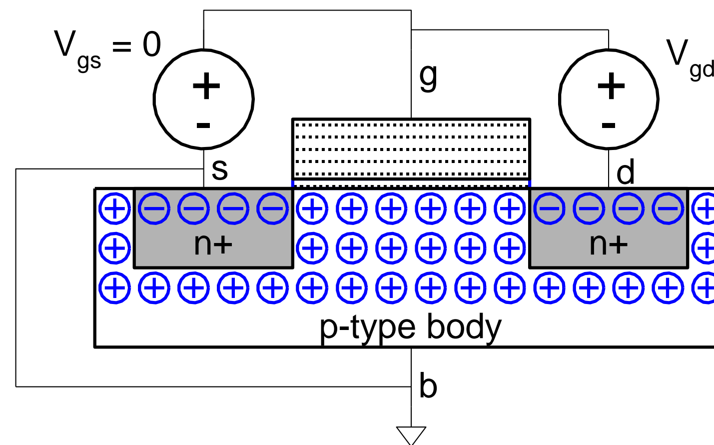
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



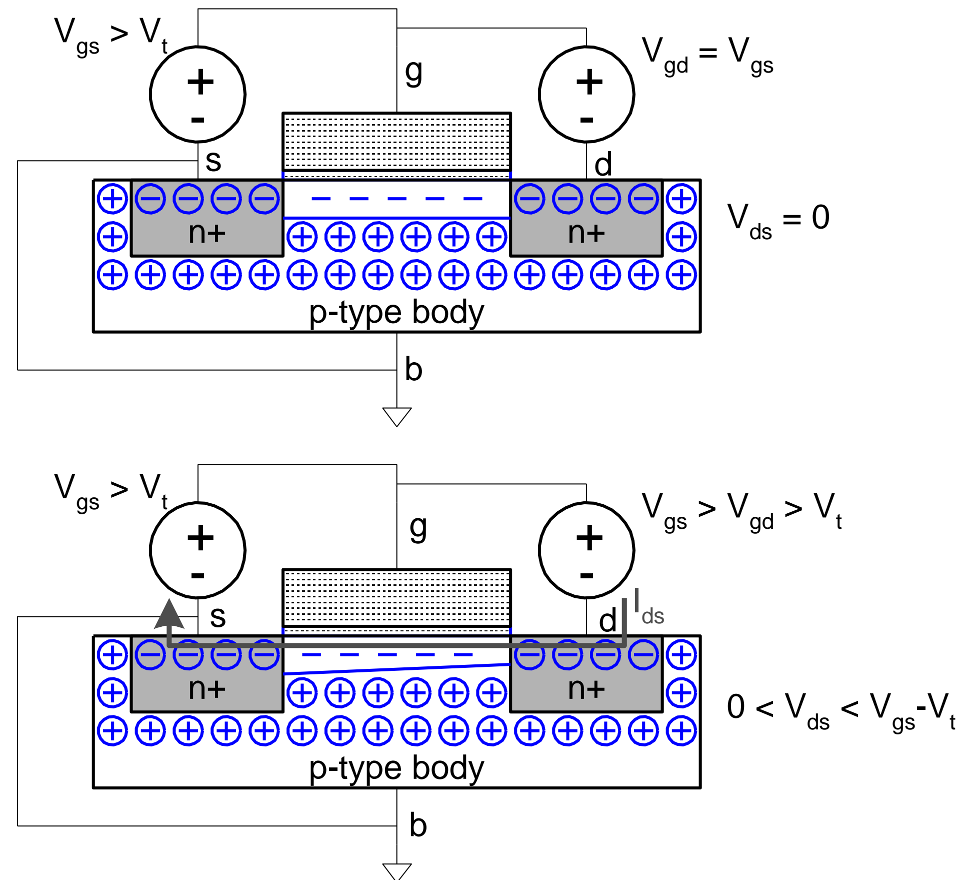
nMOS Cutoff

- No channel
- $I_{ds} \approx 0$



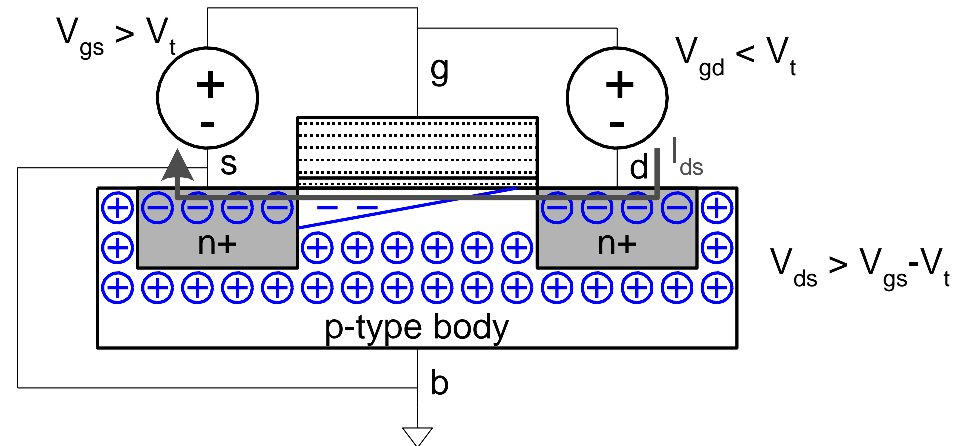
nMOS Linear

- Channel forms at both sides:
  - $V_{gs} > V_T$
  - $V_{gd} > V_T \rightarrow V_{ds} < V_{gs} - V_T$
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Increasing V_{gs}, makes channel deeper: I_{ds} increases with V_{gs}
- Similar to linear resistor



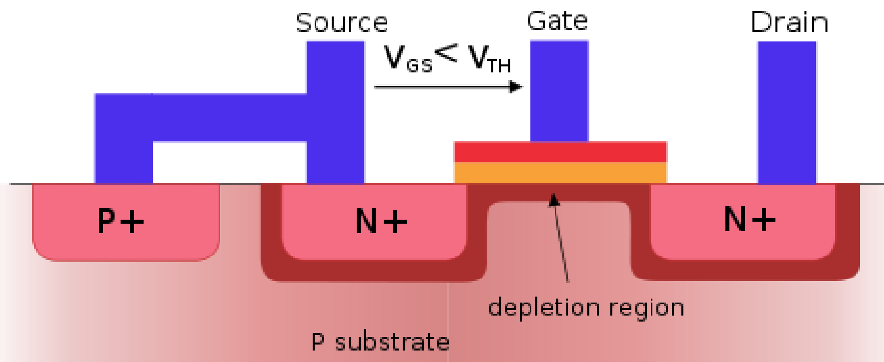
nMOS Saturation

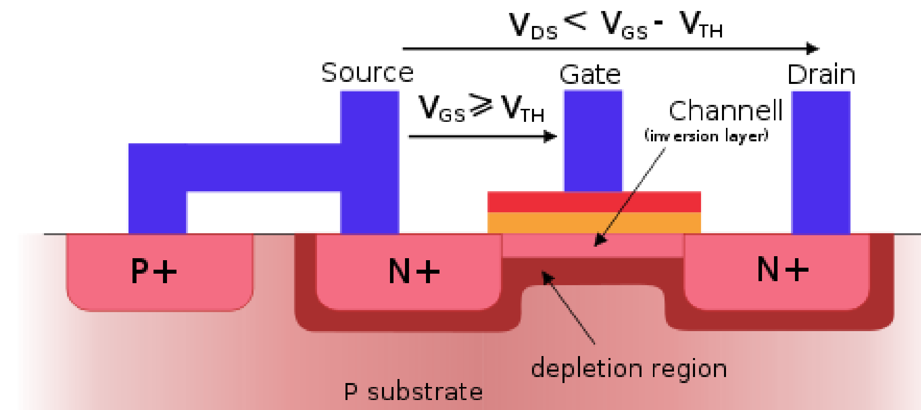
- $V_{ds} < V_{gs} - V_T$ or $V_{gd} > V_T$ no longer true
  - Channel condition not met
- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current *saturates*
- Similar to current source



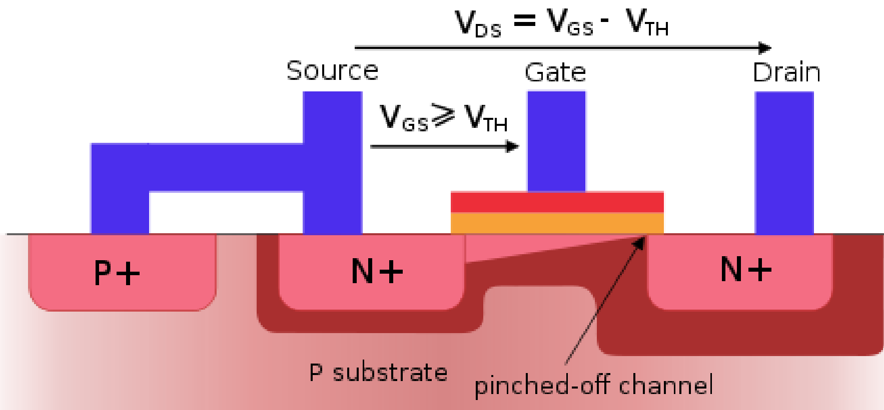
How does conduction occur after "pinch-off"? Electrons enter channel from source, then are swept across depletion region near drain by the positive drain voltage with respect to source (V_{ds}).

Resumen

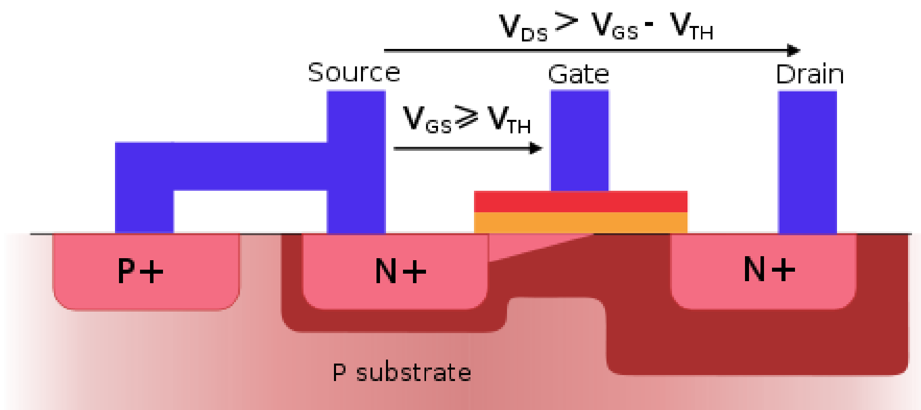




Linear operating region (ohmic mode)

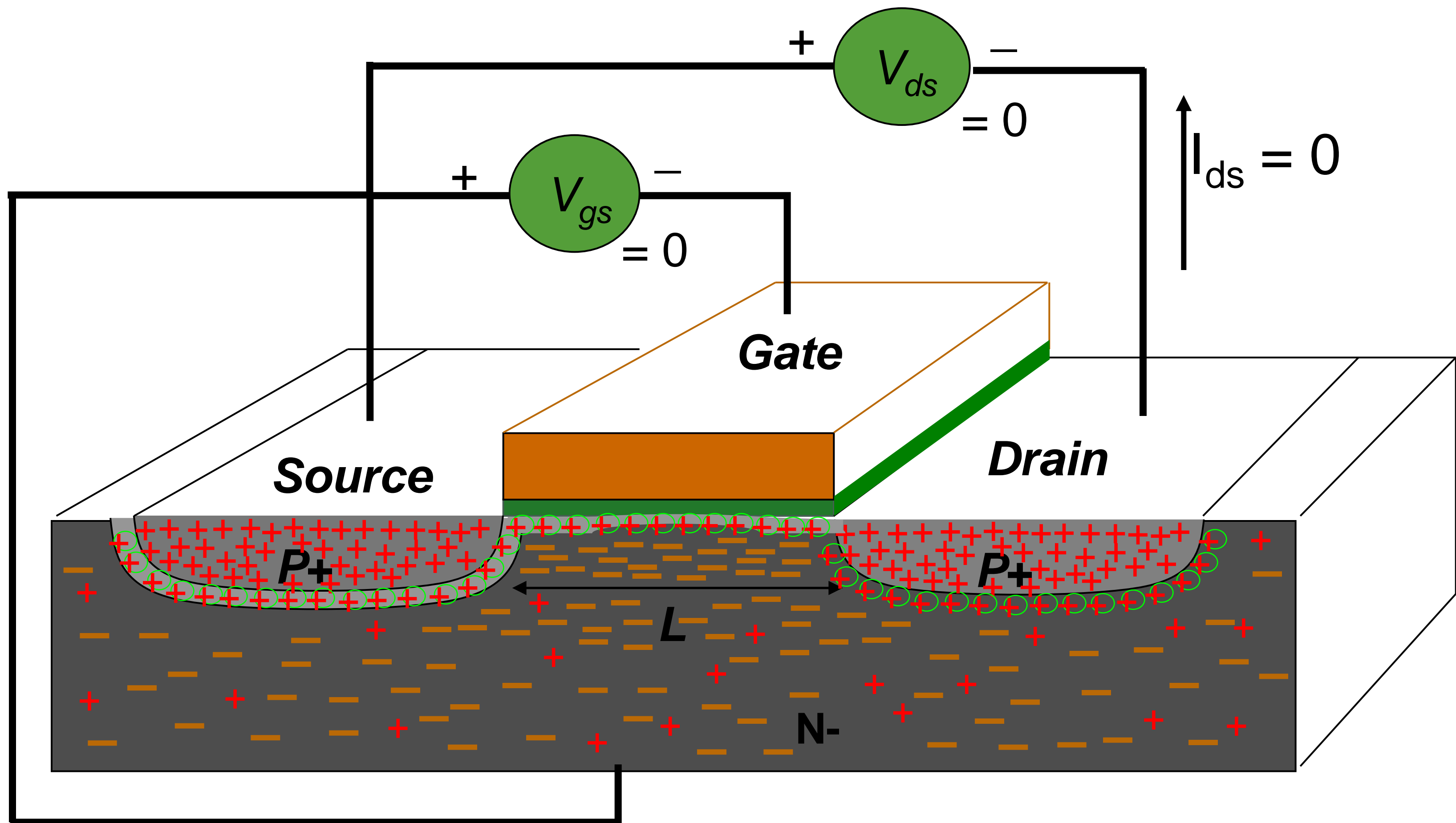


Saturation mode at point of pinch-off

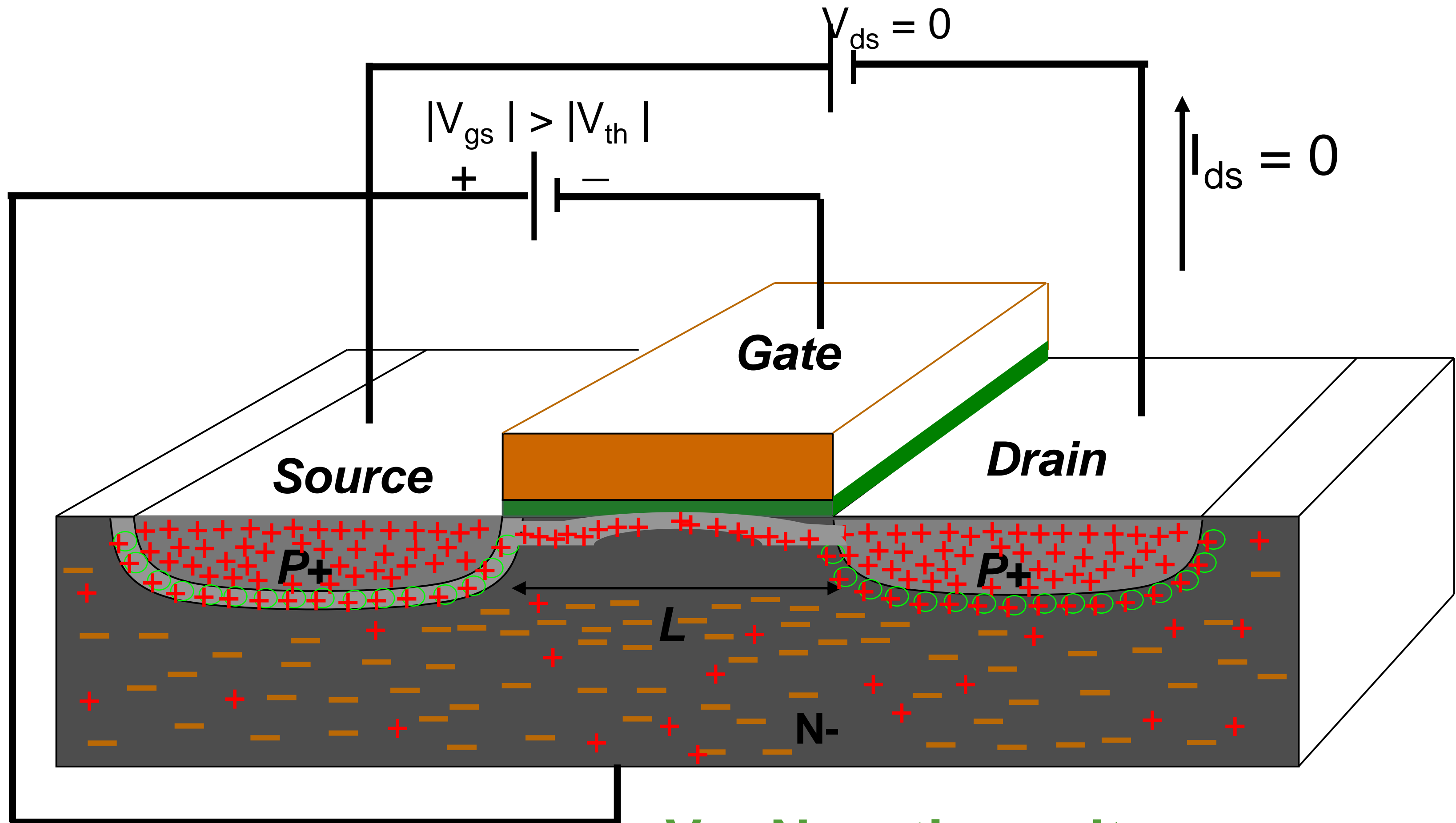


Saturation mode

PMOSFET



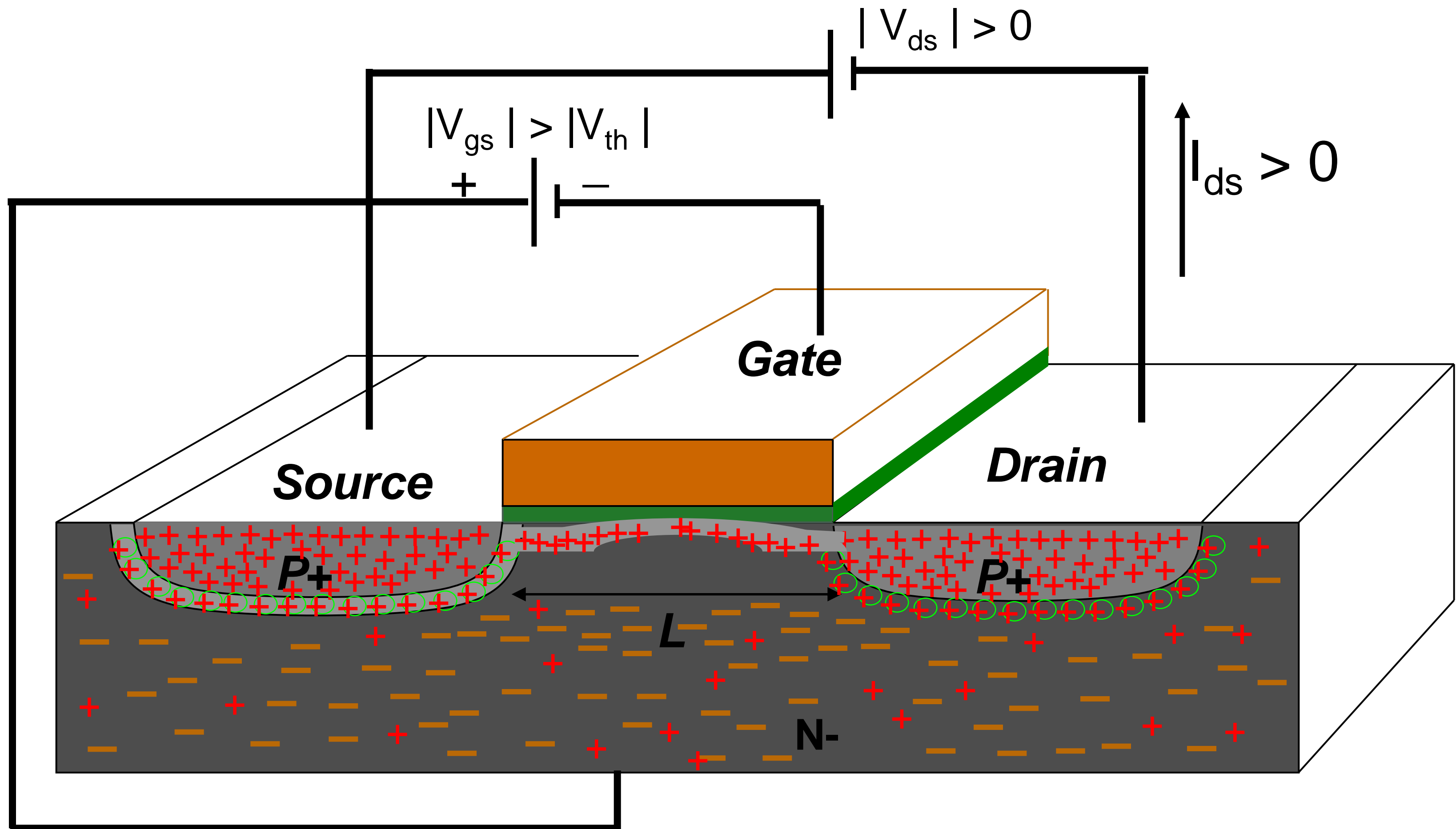
PMOSFET: No current



V_{th} Negative voltage

V_{ds} Negative voltage

PMOSFET: Current flow



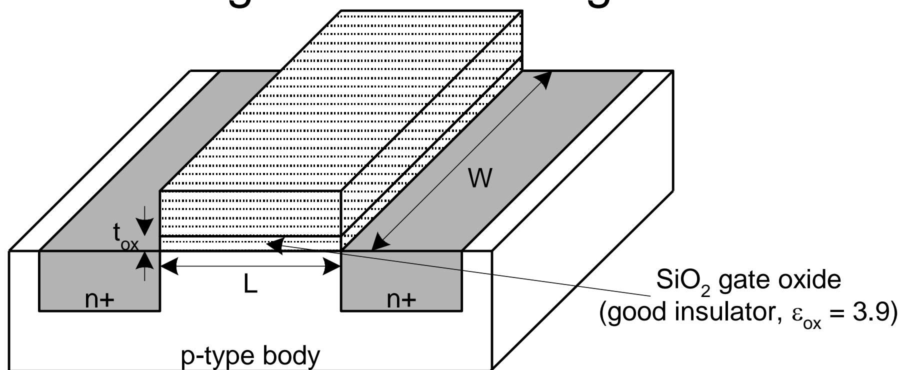
V_{gs} & V_{ds} Negative voltages

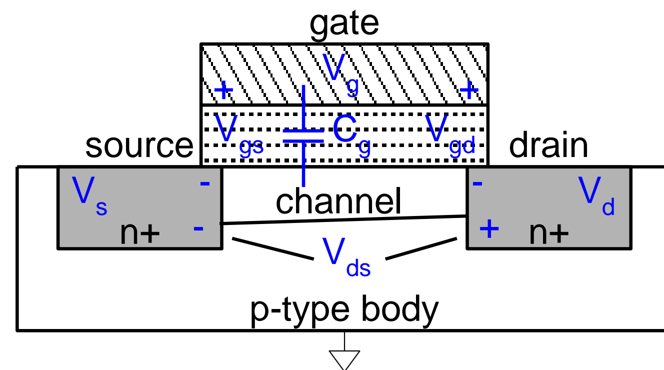
Ecuaciones del modelo ideal

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversions
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





Carrier velocity

- Charge is carried by e-
- Electrons are propelled by the lateral electric field between source and drain
  - $E = V_{ds}/L$
- Carrier velocity v proportional to lateral E-field
  - $v = \mu E$ μ called mobility
- Time for carrier to cross channel:
  - $t = L / v$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$
\begin{aligned}
I_{ds} &= \frac{Q_{channel}}{t} \\
&= \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \\
&= \beta \left(V_{gt} V_{ds} - \frac{V_{ds}^2}{2} \right)
\end{aligned}
$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

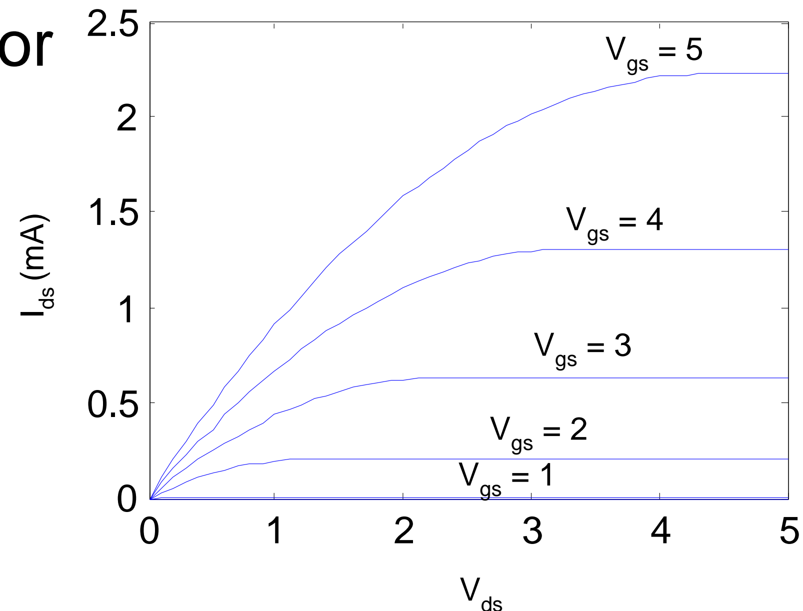
nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left(\frac{V_{gt}^2}{2} \right)$$

Example

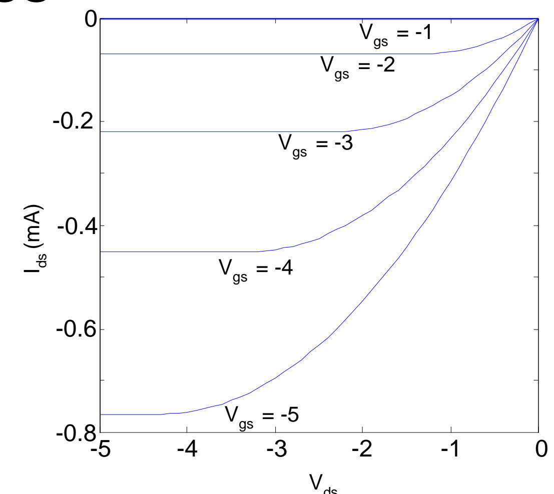
- We will be using a 0.6 μm process for your project
  - From AMI Semiconductor
  - t_{ox} = 100 Å
  - μ = 350 cm^2/V*s
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



$$\beta = \mu C_{ox} \frac{W}{L} = (350)\left(\frac{3.9 \times 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120 \frac{W}{L} \mu\text{A/V}^2$$

pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 cm^2/V•s in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

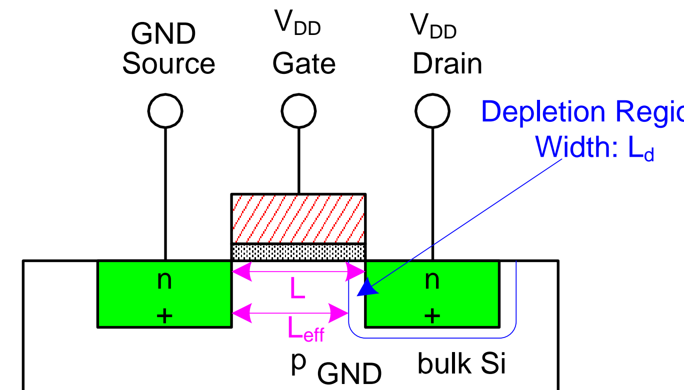


Efectos de segundo orden

- Modulación de canal
- Saturación de velocidad
- Efecto cuerpo

Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L – L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation

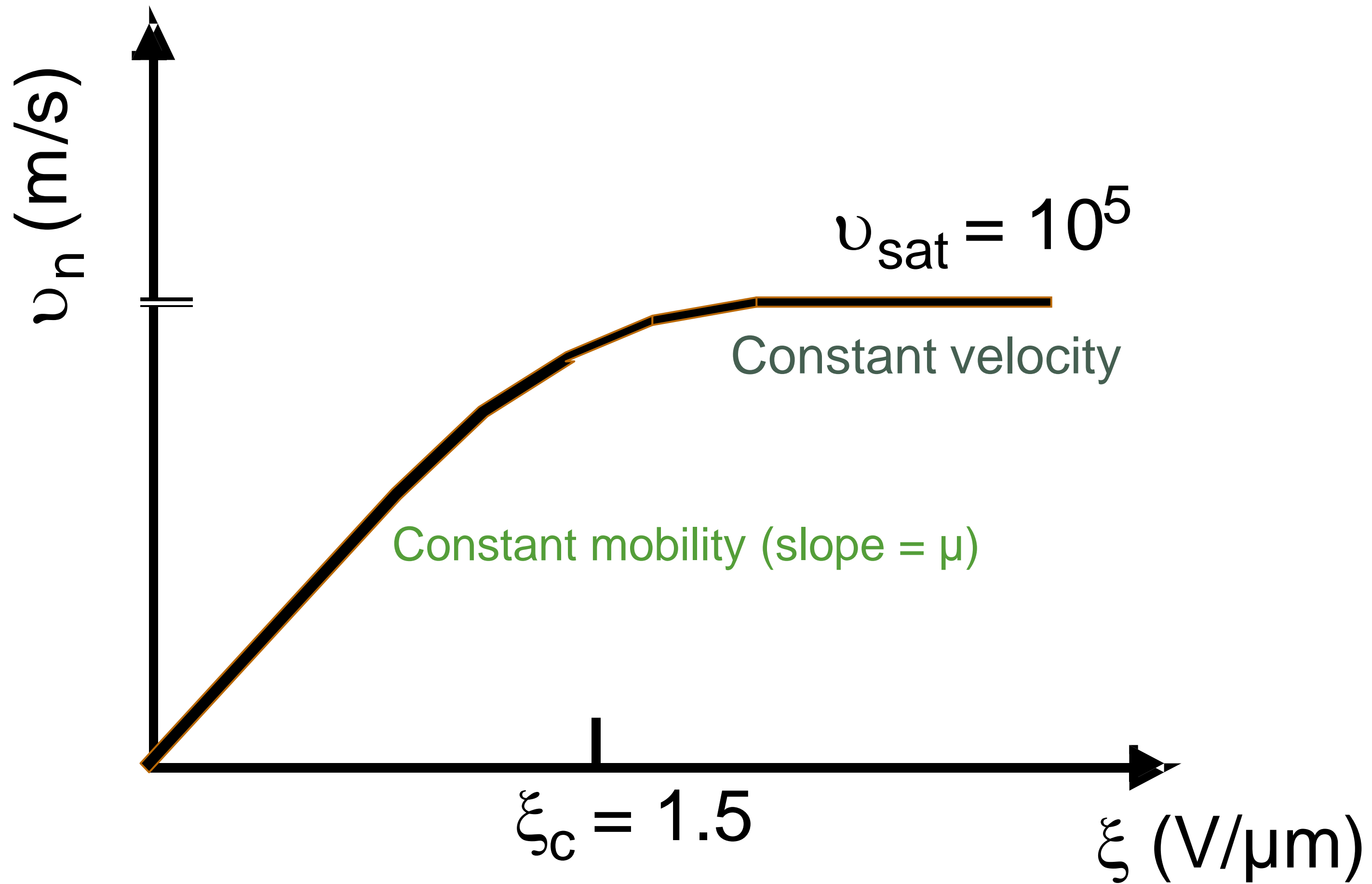


Chan Length Mod I-V

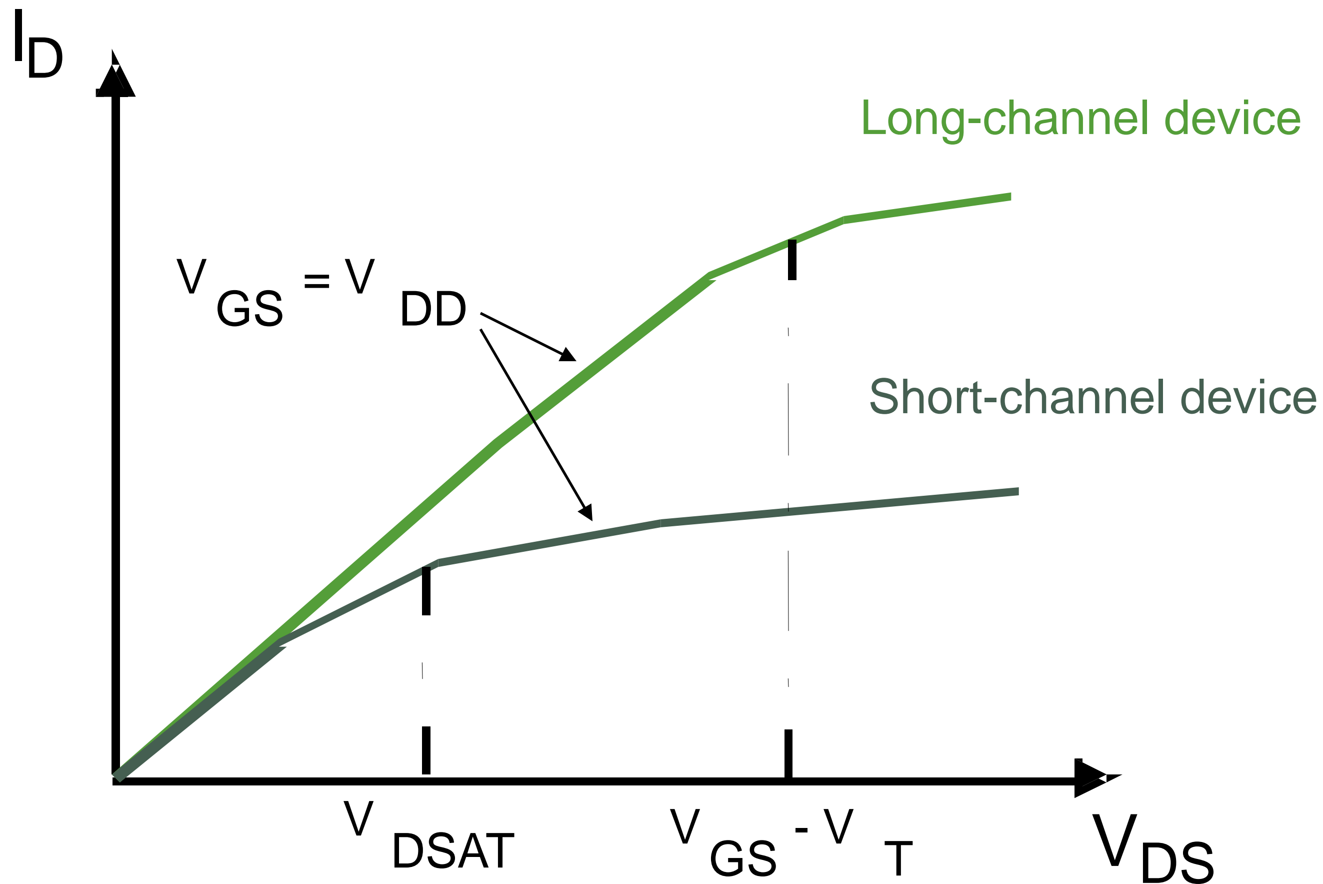
$$I_{ds} = \beta \left(\frac{V_{gt}^2}{2} \right) (1 + \lambda V_{ds})$$

- λ = *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics

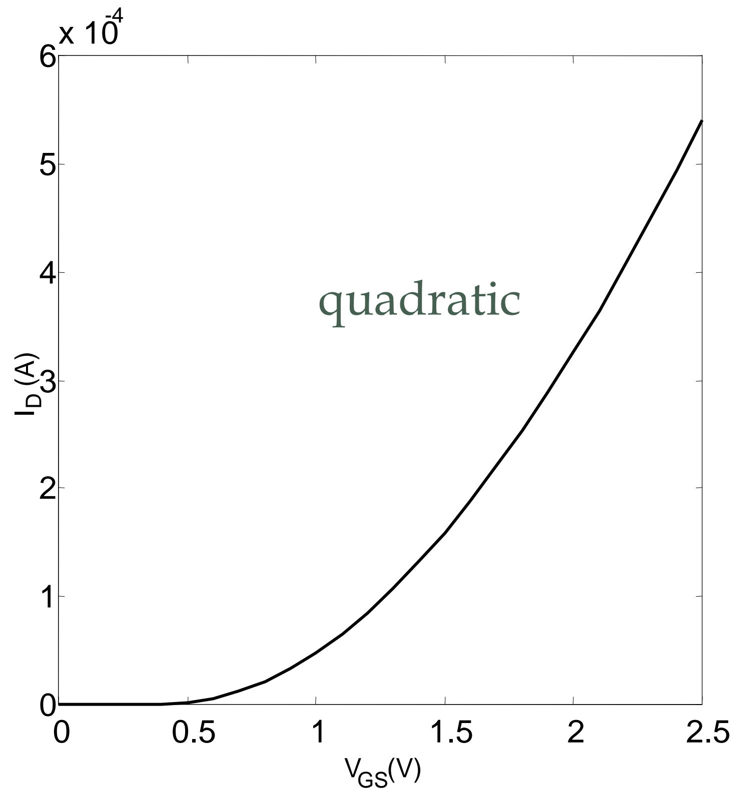
Velocity Saturation



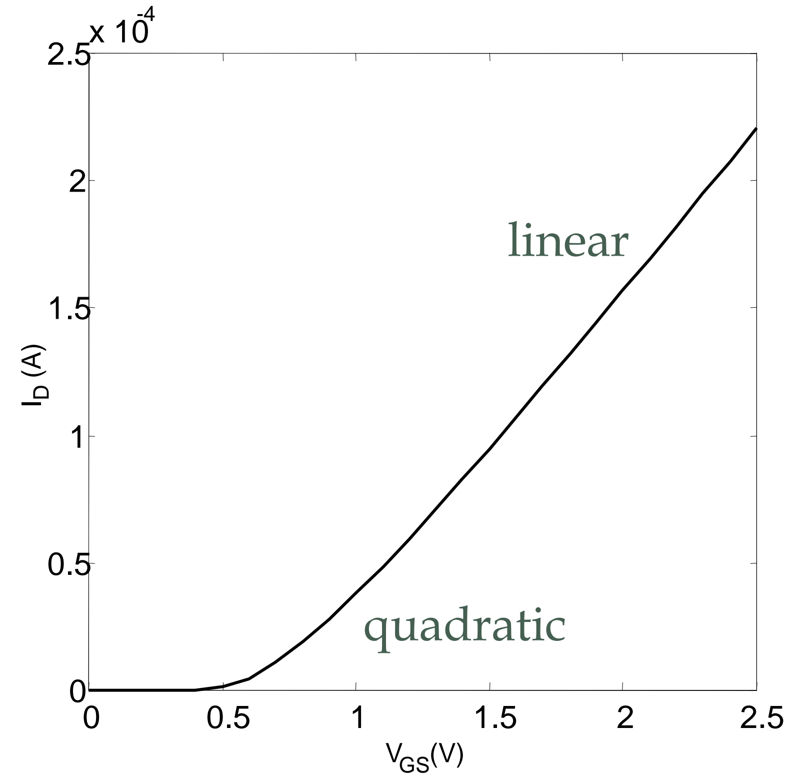
Perspective



I_D versus V_{GS}

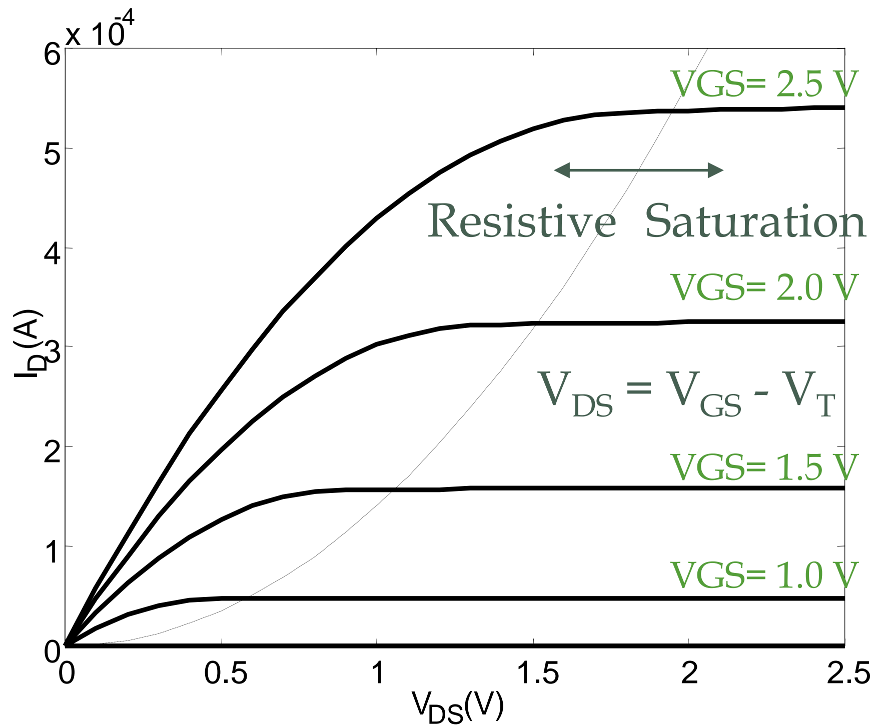


Long Channel

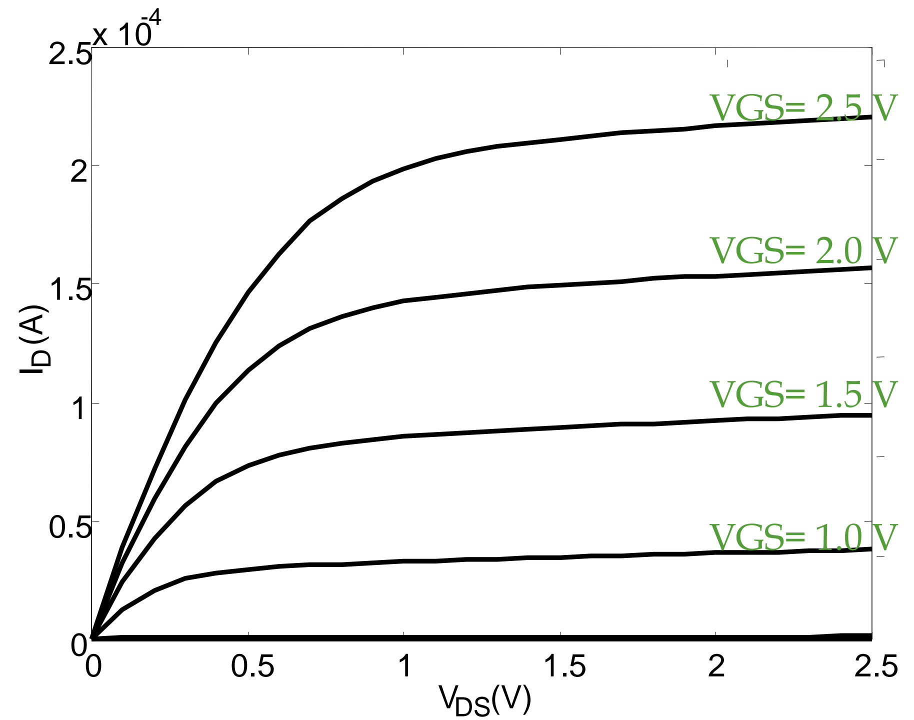


Short Channel

I_D versus V_{DS}



Long Channel

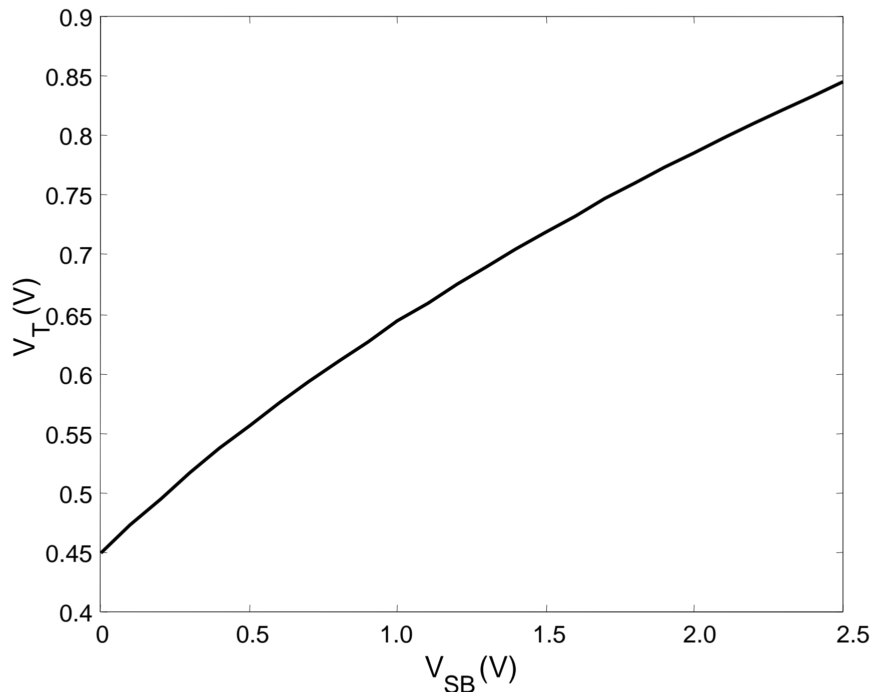


Short Channel

Body Effect

- Body is a fourth transistor terminal
- V_{sb} affects the charge required to invert the channel
  - Increasing V_s or decreasing V_b increases V_t

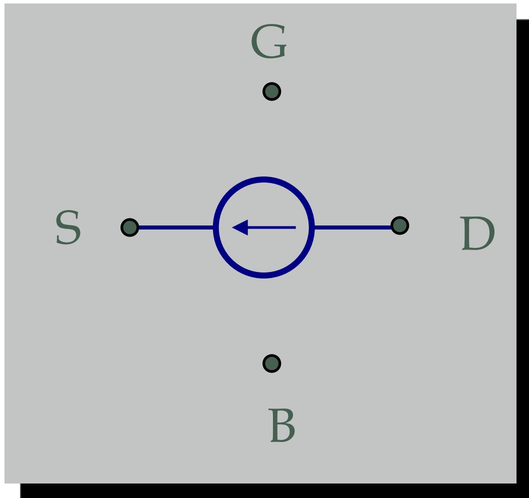
$$V_t = V_{t0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$



$V_{SB} \uparrow \rightarrow V_T \uparrow \rightarrow V_{GT} \downarrow \rightarrow I_D \downarrow$

Cuanta más diferencia haya entre la tensión de la fuente y el sustrato, menos será la corriente

A unified model for manual analysis



$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

$$\text{with } V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}),$$

$$V_{GT} = V_{GS} - V_T,$$

$$\text{and } V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Simple Model versus SPICE