ENRIQUE SEDANO

Dpto. Ingenieria Electronica
E.T.S. Ing. de Telecomunicación. Ciudad universitaria, s/n.
28040, Madrid
esedano@die.upm.es
+34 91 5495700 Ext. 4234

EDUCATION

2010 - Nowadays. Universidad Politécnica de Madrid. Ph.D., Electronic Engineering.

2008 - 2010. Universidad Complutense de Madrid. Master's Degree, Research in Computer Science.

2002 - 2008. Universidad Complutense de Madrid. Bachelor's Degree, Computer Science.

RELATED EXPERIENCE

Doctoral Scolarship, work on high-precision FPGA-based noise reduction techniques for infrared interferometers fusion diagnostics. International Programme for Attracting Talent, Campus of International Excellence, Universidad Politécnica de Madrid. January, 2011 - Nowadays.

Department internship, work on wordlength optimization techniques and noise quantization for DSP platforms. DIE department, Universidad Politécnica de Madrid. September, 2010 - December, 2011.

Department internship, work on thermal-aware compiler techniques. DACyA department, Universidad Complutense de Madrid / École Polytechnique Fédérale de Lausanne. September, 2008 - September, 2009.

Department internship, work on branch prediction schemes on FPGA platforms. DACyA department, Universidad Complutense de Madrid. October, 2007 - June, 2008.

PUBLICATIONS

International conferences

L. Esteban, J.A. López, E. Sedano y M. Sánchez, "Quantization Analysis of the Infrared Interferometer of the TJ-II for its Optimized FPGA-based Implementation", *Proceedings of IEEE 18th Real Time Conference, RTC'12, Berkeley (California, USA), June 11-15, 2012.*

E. Sedano, Juan A. López, C. Carreras, "Acceleration of Monte-Carlo simulation-based quantization of DSP systems", *International Conference on Systems, Signals and Image Processing 2012, IWSSIP 2012. April 11-13, 2012, Vienna (Austria).*

E. Sedano, Juan A. López, C. Carreras, "A Fast Interpolative Wordlength Optimization Method for DSP Systems", *VIII Southern Programmable Logic Conference, SPL 2012. March 20-23, 2012, Bento Gonçalves (Brasil).*

E. Sedano, D. Chaver, J. Resano, "Implementation of a hardware branch-predictor evaluation platform based on FPGAs", *Research in Microelectronics and Electronics, 2009. PRIME 2009. Ph.D., July 12-17, 2009, Cork (Ireland), Page(s): 44 - 47.*

J.L. Ayala, P.G. Del Valle, E. Sedano, M. Sabry, D. Atienza, "Hardware and Software Thermal-Aware Policies in Embedded Processors", *Innovative Architecture for Future Generation High-Performance Processors and Systems, International Workshop on. IWIA 2009. Kihei, Maui, Hawaii, March 16-17, 2009.*

National conferences

S. Sepulveda, E. Sedano, D. Chaver, F. Castro, L. Piñuel, F. Tirado, "Simplificación y extensión a un entorno multi-core de la política de reemplazamiento Probabilistic Escape LIFO",*CEDI 2010. July 7-10, 2010, Valencia (Spain).*

Peer reviewed journals

"Improving peLIFO replacement policy: Hardware reduction and thread-aware extension", *In peer review process.*

"Round-off noise estimation of fixed-point algorithms using polynomial chaos expansion", *In peer review process.*

Book chapters

J.A. Lopez , E. Sedano, L. Esteban, G. Caffarena, A. Fernandez-Herrero, C. Carreras, "Applications of Interval-Based Simulations to the Analysis and Design of Digital LTI Systems",*in Applications of Digital Signal Processing, ISBN 978-953-307-406-1, InTech, November 2011.*

Technical reports

E. Sedano, S. Sepulveda, D. Chaver, F. Castro, L. Piñuel, F. Tirado, "Improving PeLIFO Replacement Policy: Hardware Reduction and Thread-Aware Extension", *February 2012.*

PATENTS

Name: Systems and methods for improving the execution of computational algorithms.
Authors: Pablo Barrio López-Cortijo; Carlos Carreras Vaquer; Roberto Sierra Cabrera; Juan Antonio López Martín; Gabriel Caffarena Fernández; Enrique Sedano Algarabel; José Antonio Fernández de Blas; Ruzica Jevtic.
Main entity: Airbus Operations S.L.
Application number: 13/229.946
Prioritary country: United States of America
Date: August 12, 2011.

Name: Sistemas y métodos para mejorar la ejecución de algoritmos computacionales.
Authors: Pablo Barrio López-Cortijo; Carlos Carreras Vaquer; Roberto Sierra Cabrera; Juan Antonio López Martín; Gabriel Caffarena Fernández; Enrique Sedano Algarabel; José Antonio Fernández de Blas; Ruzica Jevtic.
Main entity: Airbus Operations S.L.
Application number: P-101100
Prioritary country: Spain
Date: May 27, 2011.

HONORS

Bachelor Project "Implementation of a HW plataform for the evaluation of branch predictors using a SPARC arquitecture" **passed with Distinction**.

Bachelor Project **awarded with Second Place** in I Edition of Premios Fin de Carrera Sun Microsystems (Bachelor Project Prizes Sun Microsystems).

Paper "Implementation of a hardware branch-predictor evaluation platform based on FPGAs" **awarded with Gold Leaf Certificate** for being among the first decile in reviewing scores.

Paper "A Fast Interpolative Wordlength Optimization Method for DSP Systems" selected for "Selected Papers from SPL 2012" special issue of Int. Journal of Reconfigurable Computing (IJRC).

EMPLOYMENT

Teacher, Automaton Theory and Finite Languages, at Intecysa School (Aramaia S.L.). July, 2006 - August 2008.

TECHNICAL SKILLS

Programming languages (skill)

C/C++ (High), VHDL (High), Java (Intermediate), Verilog (Intermediate), Prolog (Intermediate), MySQL (Intermediate), Haskell (Beginner), Motorola 68000 assembly (Intermediate),

Pascal (Intermediate / Beginner)

Operative systems (skill)
Microsoft Windows XP/Vista/7/Me/2000 (User/Admin), Linux Ubuntu/SuSe (Intermediate user)

Programming tools and environments
Xilinx ISE, Xilinx EDK, ModelSim, OrCAD, Eclipse, NetBeans, gcc, JBuilder, C++ Builder, Matlab, Octave, Pspice, LaTeX.

LANGUAGES

Spanish, mother tongue.

English, C1 level. CAE Certification.

French, A1 level.

PROFESSIONAL AFFILIATIONS

European Network of Excellence on High Performance and Embedded Architecture and Compilation.

OTHER SKILLS

Organisational skills
Leadership (Vice-president from 2005 to 2007, and president from 2007 to 2008 of Student's Delegation. Vice-president of RITSI association from 2005 to 2007). Ability to communicate. Experience in proyect management. Capacity of innovation, fast-learning and adaptation.

Social skills
Teamwork. Ability to adapt to multicultural environments. Assertiveness. Creativity.

Technical and academical revision
Reviewer of papers for EURASIP Journal of Embedded Systems, ISSN 1687-3955, Hindawi Publishing (2010).

Reviewer of papers for VII Southern Conference on Programmable Logic (2010).

Reviewer of papers for DASIP 2012 (Design & Architectures for Signal & Image Processing, Conference on).